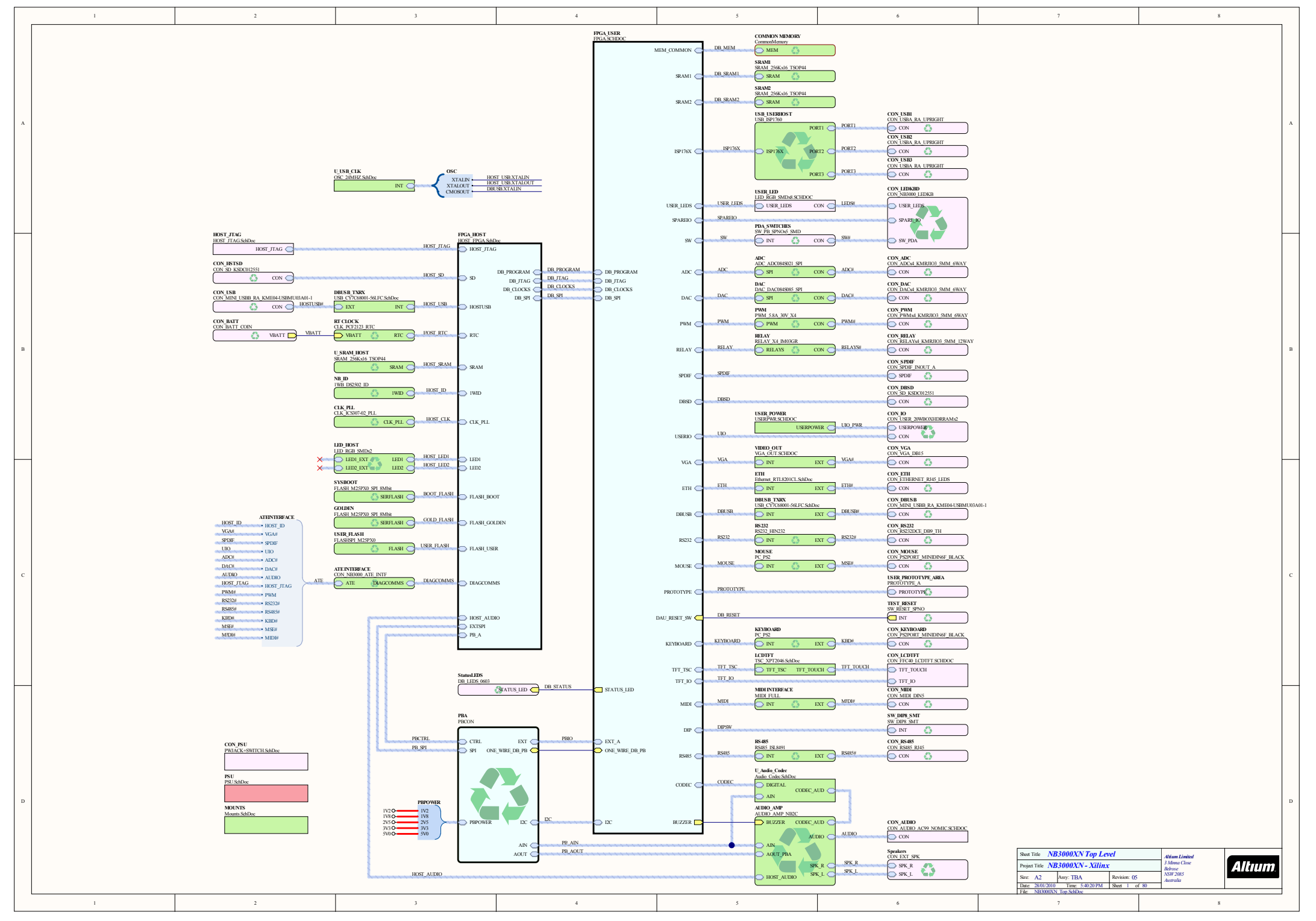
FPGA_USER
FPGA.SCHDOC
COMMON MEMORY
CommonMemory
SRAM1
SRAM_256Kx16_TSOP44
SRAM2
SRAM_256Kx16_TSOP44
USB_USERHOST
USB_ISP1760
CON_USB1
CON_USBA_RA_UPRIGHT
CON_USB2
CON_USBA_RA_UPRIGHT
CON_USB3
CON_USBA_RA_UPRIGHT
USER_LED
LED_RGB_SMDx8.SCHDOC
CON_LEDKBD
CON_NB3000_LEDKB
PDA_SWITCHES
SW_PB_SPNOx5_SMD
ADC
ADC_ADC0845021_SPI
CON_ADCx4_KMRJIO3_5MM_6WAY
DAC
DAC_DAC0845085_SPI
CON_DACx4_KMRJIO3_5MM_6WAY
PWM
PWM_5.8A_36V_X4
CON_PWMx4_KMRJIO3_5MM_6WAY
RELAY
RELAY_X4_IM03GR
CON_RELAYx4_KMRJIO3_5MM_12WAY
CON_SPDIF
CON_SPDIF_INOUT_A
CON_DBSD
CON_SD_KSDC012551
USER_POWER
USERPWR.SCHDOC
CON_IO
CON_USER_20WIOXHDRRAMx2
VIDEO_OUT
VGA_OUT.SCHDOC
CON_VGA
CON_VGA_DB15
ETH
Ethernet_RTL8201CL.SchDoc
CON_ETH
CON_ETHERNET_RJ45_LEDS
DBUSB_TXRX
USB_CY7C68001-56LFC.SchDoc
CON_DBUSB
CON_MINI_USBB_RA_KME04-USBM.U03A01-1
RS232
RS232_HIN232
CON_RS232
CON_RS232DCE_DB9_TH
MOUSE
PC_PS2
CON_MOUSE
CON_PS2PORT_MINIDIN6F_BLACK
USER_PROTOTYPE_AREA
PROTOTYPE_A
TEST_RESET
SW_RESET_SPNO
KEYBOARD
PC_PS2
CON_KEYBOARD
CON_PS2PORT_MINIDIN6F_BLACK
LCDTFT
TSC_XPT2046.SchDoc
CON_LCDTFT
CON_FFC40_LCDTFT.SCHDOC
MIDI INTERFACE
MIDI_FULL
CON_MIDI
CON_MIDI_DIN5
SW_DIP8_SMT
RS485
RS485_ISL8491
CON_RS485
CON_RS485_RJ45
U_Audio_Codec
Audio_Codec.SchDoc
AUDIO_AMP
AUDIO_AMP_NB2C
CON_AUDIO
CON_AUDIO_AC99_NOMIC.SCHDOC
Speakers
CON_EXT_SPK
U_USB_CLK
OSC_24MHZ.SchDoc
OSC
HOST_JTAG
HOST_JTAG.SchDoc
CON_HSTSD
CON_SD_KSDC012551
CON_USB
CON_MINI_USBB_RA_KME04-USBM.U03A01-1
CON_BATT
CON_BATT_COIN
RT CLOCK
CLK_PCF2123_RTC
U_SRAM_HOST
SRAM_256Kx16_TSOP44
NB_ID
1WB_DS2502_ID
CLK_PLL
CLK_ICS307-02_PLL
LED_HOST
LED_RGB_SMDx2
SYSBOOT
FLASH_M25PX0_SPI_8Mbit
GOLDEN
FLASH_M25PX0_SPI_8Mbit
USER_FLASH
FLASHSPI_M25PX0
ATE INTERFACE
CON_NB3000_ATE_INTF
FPGA_HOST
HOST_FPGA.SchDoc
ATEINTERFACE
StatusLEDS
DB_LEDS_0603
PBA
PBCON
PBPOWER
CON_PSU
PWJACK+SWITCH.SchDoc
PSU
PSU.SchDoc
MOUNTS
Mounts.SchDoc
Sheet Title NB3000XN Top Level
Project Title NB3000XN - Xilinx
Size: A2
Assy: TBA
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Sheet 1 of 80
File: NB3000XN_Top.SchDoc
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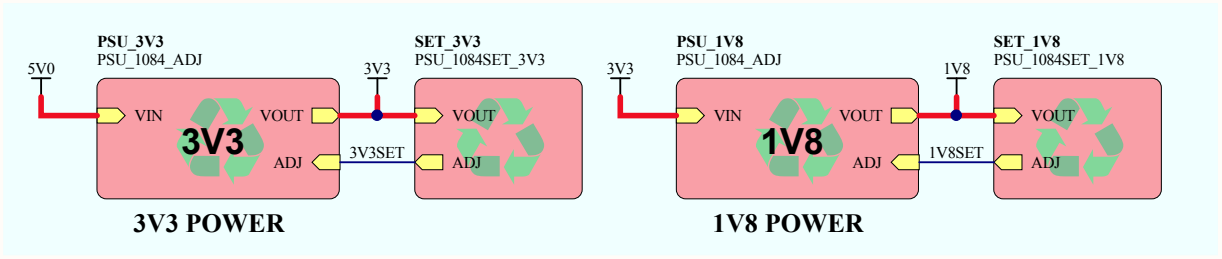
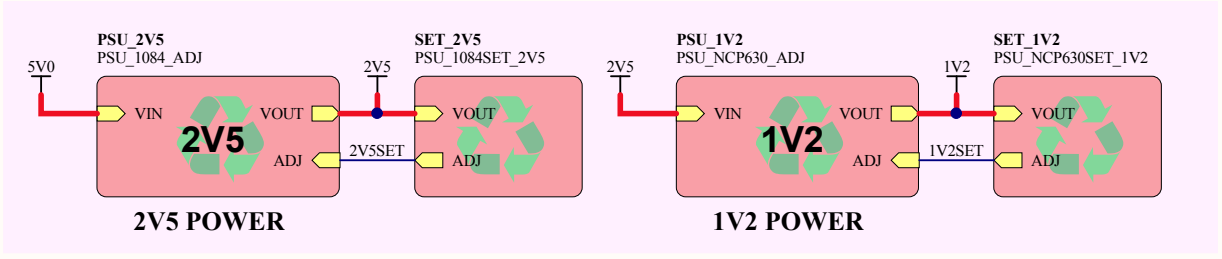
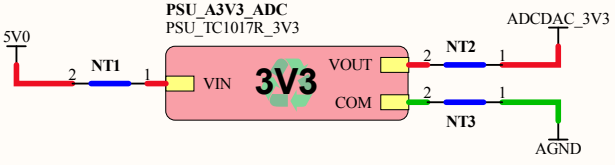
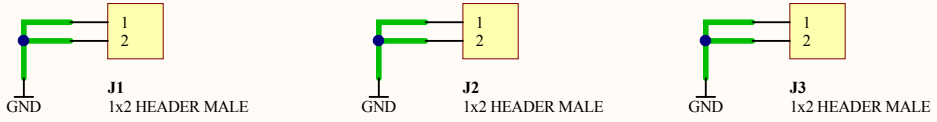
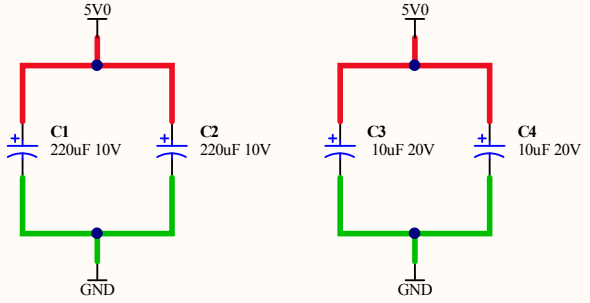


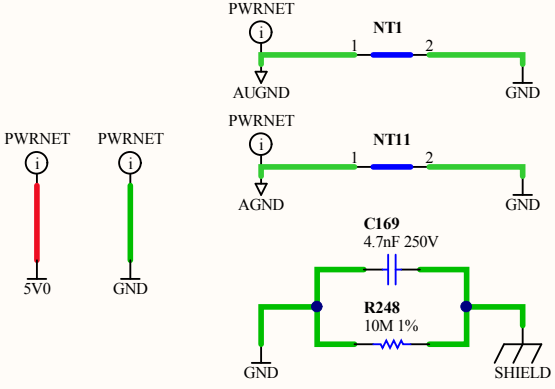


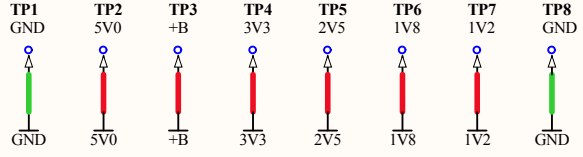




GROUND TEST POINTS







POWER TEST POINTS

Sheet Title	NB3000 POWER SUPPLIES		
Project Title	NB3000XN - Xilinx		
Size: A4	Assy: TBA	Revision: 05	
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File: PSU.SchDoc			

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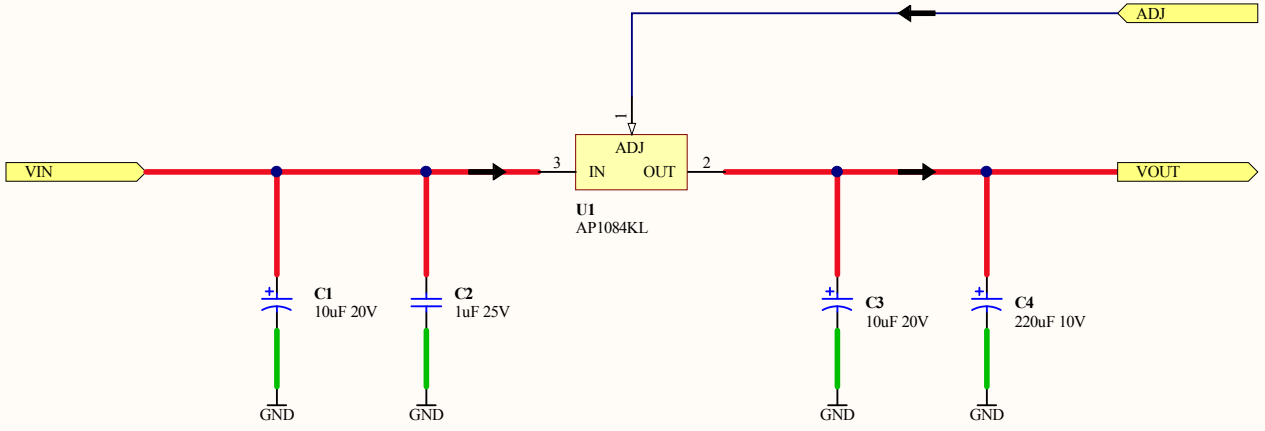

Sheet Title	*PSU AP1084KL ADJ*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:20 PM	Sheet 3 of 80	
File: PSU_1084_ADJ.SchDoc			

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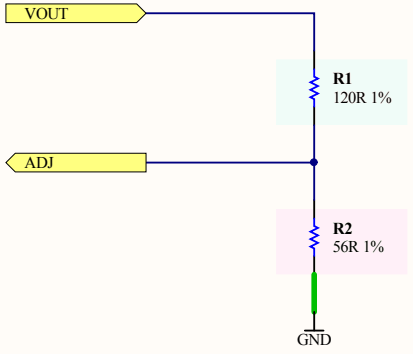
1.8V Output



$$V_{out} = V_{REF}\left\{1+\frac{R2}{R1}\right\} + I_{ADJ}R_2$$

V_{REF} = 1.25v

I_{ADJ} = 55uA (0.000055)

Calculation for 1.8V;

= 1.25V x (1+R2/R1) + 0.000055 x R2

= 1.25V x (1+56/120) + 0.000055 x 56

= 1.25V x 1.47 + 0.00308

= 1.83641V

Sheet Title	*PSU AP1084KL 1V8*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:20 PM	Sheet 4 of 80	
File: PSU_1084SET_1V8.SchDoc			

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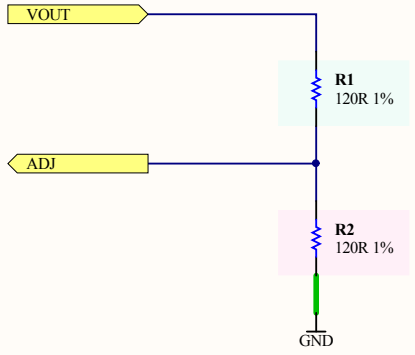
2.5V Output



$$V_{out} = V_{REF}\left\{1+\frac{R2}{R1}\right\} + I_{ADJ}R_2$$

V_{REF} = 1.25v

I_{ADJ} = 55uA (0.000055)

Calculation for 2.5V;

= 1.25V x (1+R2/R1) + 0.000055 x R2

= 1.25V x (1+120/120) + 0.000055 x 120

= 1.25V x 2 + 0.0066

= 2.50066V

Sheet Title	*PSU AP1084KL SET TO 2V5*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:20 PM	Sheet 5 of 80	
File: PSU_1084SET_2V5.SchDoc			

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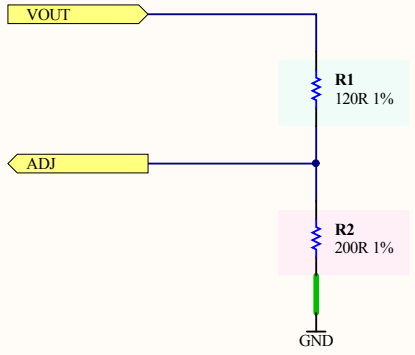
3.3V Output



$$V_{out} = V_{REF}\left\{1+\frac{R2}{R1}\right\} + I_{ADJ}R_2$$

V_{REF} = 1.25v

I_{ADJ} = 55uA (0.000055)

Calculation for 3.3V;

= 1.25V x (1+R2/R1) + 0.000055 x R2

= 1.25V x (1+200/120) + 0.000055 x 200

= 1.25V x 2.67 + 0.011

= 3.34433V

Sheet Title	*PSU AP1084KL SET TO 3V3*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:20 PM	Sheet 6 of 80	
File: PSU_1084SET_3V3.SchDoc			

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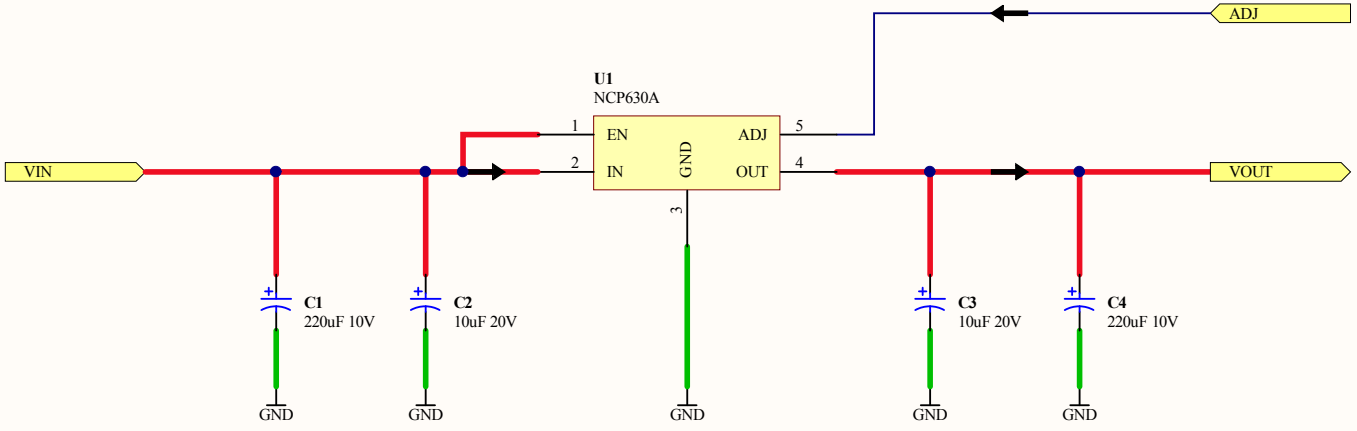

Sheet Title	***PSU NCP630A ADJ***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:20 PM	Sheet 7 of 80	
File: PSU_NCP630_ADJ.SchDoc			

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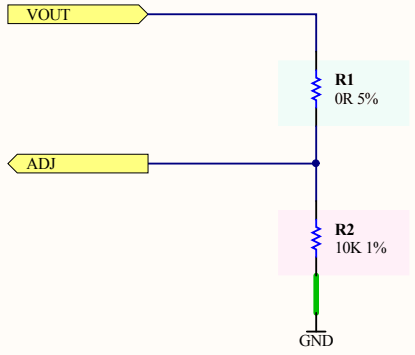
1.2V Output



$$V_{out} = V_{REF}\left\{1+\frac{R1}{R2}\right\} + I_{ADJ}\,R_2$$

V_{REF} = 1.216v

I_{ADJ} = 40nA (0.000000040)

Calculation for 1.2V;

= 1.216V x (1+R1/R2) + 0.000000040 x R2

= 1.216V x (1+0/10000) + 0.000000040 x 10000

= 1.216V x 1 + 0.0004

= 1.2164V

Sheet Title	*PSU NCP630A SET TO 1V2*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:20 PM	Sheet 8 of 80	
File: PSU_NCP630SET_1V2.SchDoc			

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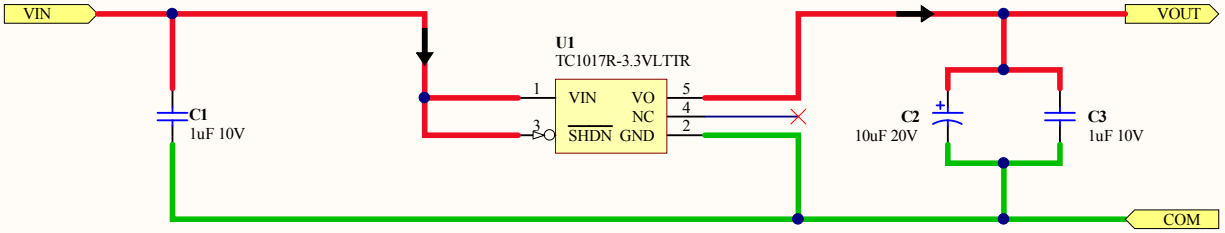
3V3

150mA
50uVRMS



Sheet Title	*PSU TC1017R 3V3*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:20 PM	Sheet 9 of 80	
File: PSU_TC1017R_3V3.SchDoc			

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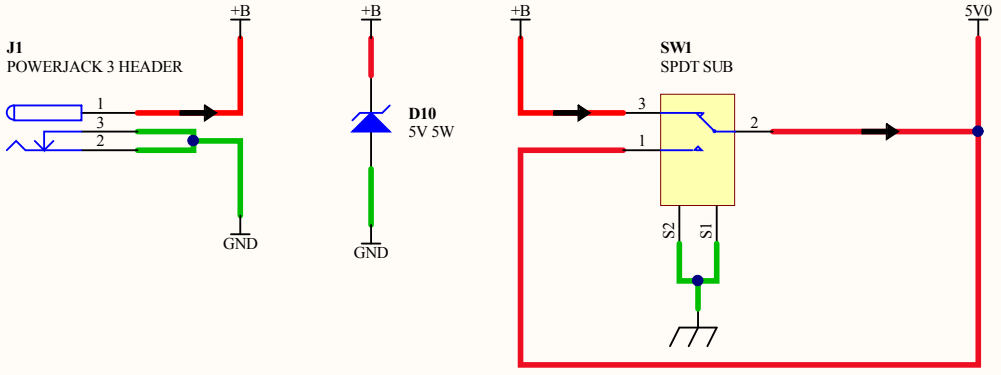

Sheet Title	***Power Jack & Switch***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
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File: PWJACK+SWITCH.SchDoc			

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SYSTEM CLOCKS

CLK_PLL
SCLK
CS_N
DIN
CLK_FIXED
CLK_PROG
CLKGEN_SCLK
CLKGEN_CS_N
CLKGEN_DIN
REF_CLK
FPGA_CLK

USER FPGA CLOCKS

DB_CLOCKS
REF_CLK
FPGA_CLK
FPGA_CLK1
DB_CLK1
R1_HOST
5R6 1%

HOST RTC

RTC
CS_N
SCLK
DOUT
DIN
CLKOE
CLKOUT
INT_N
RTC_CS
RTC_SCLK
RTC_DOUT
RTC_DIN
CLKOE
CLKOUT
RTC_INT_N

ONE WIRE ID

1WID
DATA
EXT_PROG
ONE_WIRE_ID

HOST AUDIO - Delta-Sigma

HOST_AUDIO
STEREO
L
R
AOUT_L
AOUT_R

USER FPGA JTAG

DB_JTAG
HARDSOFT_JTAG
HARD
SOFT
TDI
TCK
TMS
TDO
FPGA_TDI
FPGA_TCK
FPGA_TMS
FPGA_TDO
NEXUS_TDI
NEXUS_TCK
NEXUS_TMS
NEXUS_TDO

USER FPGA PROGRAM

DB_PROGRAM
DAU_CTRL
DIN
DONE
INSTALLED
ID[3..0]
CCLK
PROGRAM
M[2..0]
INIT
PROG_PWR_ON
PROG_CLK
FPGA_DIN
FPGA_DONE
FPGA_ID[3..0]
FPGA_CCLK
FPGA_PROGRAM
FPGA_M[2..0]
FPGA_INIT
FPGA_PROG_PWR_ON
FPGA_PROG_CLK

HOST USB

USB2
HOSTUSB
USB_INTF
READY
INT_N
FLAGA
FLAGB
FLAGC
VBUS
WR_N
RD_N
D[15..0]
RESET_N
SLOE
FIFOADR2
FIFOADR0
FIFOADR1
PKTEND
FLAGD_CS_N
IFCLK
XTALIN
XTALOUT
HUSB_READY
HUSB_INT_N
HUSB_FLAGA
HUSB_FLAGB
HUSB_FLAGC
HUSB_VBUS
HUSB_WR_N
HUSB_RD_N
HUSB_D[15..0]
HUSB_RESET_N
HUSB_SLOE
HUSB_FIFOADR2
HUSB_FIFOADR0
HUSB_FIFOADR1
HUSB_PKTEND
HUSB_FLAGD_CS_N
HUSB_IFCLK
USB_XTALIN
USB_XTALOUT

PB SPI

EXTSPI
DOUT
DIN
SCLK
EXTSPI_DOUT
EXTSPI_DIN
EXTSPI_SCLK

PB - Control

PB_A
PBCTRL
JTAG
HARD
SOFT
DETECT
CLK
1W
SPARE[1..4]
SPI_CS_N[1..0]
TDI
TDO
TCK
TMS
AUTO_TDI_HARD
AUTO_TDO_HARD
AUTO_TCK_HARD
AUTO_TMS_HARD
AUTO_TDI_SOFT
AUTO_TDO_SOFT
AUTO_TCK_SOFT
AUTO_TMS_SOFT
AUTO_JTAG
EN
CLK[2..0]
CLK_ENA
CLK_EXTA[2..0]
ID
PIO[1..2]
ONE_WIRE_PB_ID_A
ONE_WIRE_PIOA[1..2]
PB_SPARE[1..4]
EXTSPI_CSN_N[1..0]

SRAM - 64K/256K x 16

SRAM
SRAM-256Kx16
A[18..0]
D[15..0]
NCS
NWE
NOE
NBHE
NBLE
SRAM_A[18..0]
SRAM_D[15..0]
SRAM_NCS
SRAM_NWE
SRAM_NOE
SRAM_NBHE
SRAM_NBLE

USER 8MB SPI FLASH x2

FLASH_USER
SERIALFLASH
FLASH2_CS_N
DIN
DOUT
SCLK
FLASH1_CS_N
USERFLASH2_CS_N
USERFLASH1_DIN
USERFLASH1_DOUT
USERFLASH1_SCLK
USERFLASH1_CS_N

SYSBOOT

FLASH_BOOT
SERFLASH
FLASH_CS_N
DOUT
DIN
SCLK
FLASH_BOOT_CS_N
FLASH_BOOT_DOUT
FLASH_BOOT_DIN
FLASH_BOOT_CLK

HOST JTAG

HOST_JTAG
HARDSOFT_JTAG
HARD
SOFT
TDI
TMS
TCK
TDO
HOST_HARD_TDI
HOST_HARD_TMS
HOST_HARD_TCK
HOST_HARD_TDO
HOST_SOFT_TMS
HOST_SOFT_TCK
HOST_SOFT_TDI
HOST_SOFT_TDO
HOST_NonIO
Host_FPGA_NonIO.SchDoc

USER FPGA SPI

DB_SPI
CLK
DIN
DOUT
MODE
SEL
DAU_SPI_CLK
DAU_SPI_DOUT
DAU_SPI_DIN
DAU_SPI_MODE
DAU_SPI_SEL

HOST SD CARD

SD
DAT[3..0]
CMD
CLK
DETECT
PROTECT
SD_DAT[3..0]
SD_CMD
SD_CLK
SD_DETECT
SD_PROTECT

Host LEDs

LED1
LED2
RGB_LED
RED
GREEN
BLUE
LED1_RED
LED1_GREEN
LED1_BLUE
LED2_RED
LED2_GREEN
LED2_BLUE

GOLDEN

FLASH_GOLDEN
SERFLASH
FLASH_CS_N
DOUT
DIN
SCLK
FLASH_GOLD_CS_N
FLASH_GOLD_DOUT
FLASH_GOLD_DIN
FLASH_GOLD_CLK

DIAGCOMMS
FLASH_CS_N
DOUT
DIN
SCLK
DIAG_CS_N
DIAG_DOUT
DIAG_DIN
DIAG_CLK

PLATFORM UPGRADE

HOST_M1
GND
J1
1x2 HEADER MALE

U1A
XC3S400AN-4FGG400C
BANK 0

U1B
XC3S400AN-4FGG400C
BANK 1

U1C
XC3S400AN-4FGG400C
BANK 2

U1D
XC3S400AN-4FGG400C
BANK 3

U1E
XC3S400AN-4FGG400C

HSWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP HIGH= INT PULLUPS OFF
HSWAP LOW= INT PULLUPS ON

XC3S1400AN MODE PIN CONFIGURATIONS

M2	M1	M0	FUNCTION
0	0	0	PLATFORM FLASH MODE
0	0	1	SPI MODE (MASTER)
0	1	0	BYTE PARALLEL INTERFACE
0	1	1	INTERNAL MASTER SPI FLASH
1	0	0	<RESERVED>
1	0	1	JTAG MODE
1	1	0	SLAVE PARALLEL
1	1	1	SLAVE SERIAL

M0 (INT PULL UP VIA HSWAP)
START ADD= 0x00_0000 INCREMENTING
START ADD= 0xFF_FFFF DECREMENTING

M1 (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG

M2 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG

XC3S1400AN SPI MODE CONFIGURATIONS

VS2	VS1	VS0	FUNCTION
0	0	0	<RESERVED>
0	0	1	<RESERVED>
0	1	0	<RESERVED>
0	1	1	<RESERVED>
1	0	0	<RESERVED>
1	0	1	(0x03) STANDARD READ
1	1	0	(0x0B) READ ARRAY
1	1	1	**(0x0B) SPI FAST READ**

VS0 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO 2

VS1 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO 2

VS2 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B) — VCCO 2

PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG

DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG

HOST_M0 R1 2K2 1% 3V3
HOST_M1 R2 2K2 1% 3V3
HOST_M2 R3 2K2 1% GND
HOST_VS0 R269 2K2 1% 3V3
HOST_VS1 R270 2K2 1% 3V3
HOST_VS2 R271 2K2 1% 3V3
DIAG_CS_N R99 2K2 1% 3V3

1V2

HOST_DECOUPLING_CAPS_1V2
FPGA_Bypass_1V2.SCHDOC

3V3

HOST_DECOUPLING_CAPS_3V3
FPGA_Bypass_3V3.SCHDOC

Sheet Title	Host Controller - Spartan3AN-400		
Project Title	NB3000XN - Xilinx		
Size: A2	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:21 PM	Sheet 11 of 80	
File: Host_FPGA.SchDoc			

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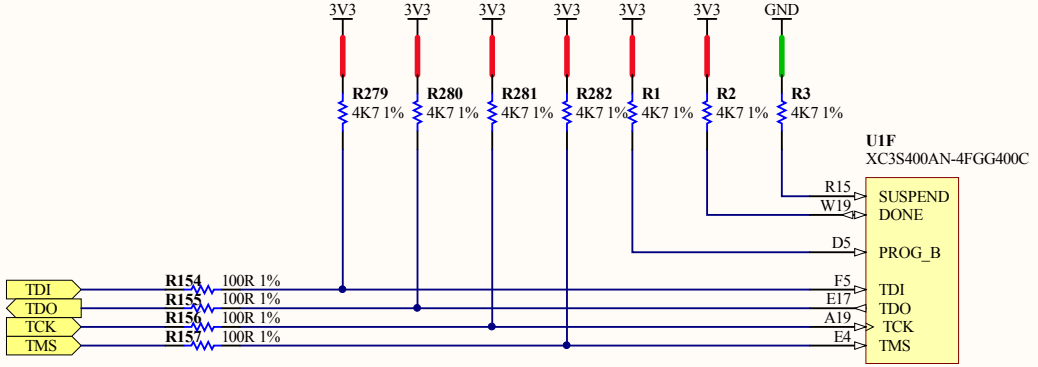

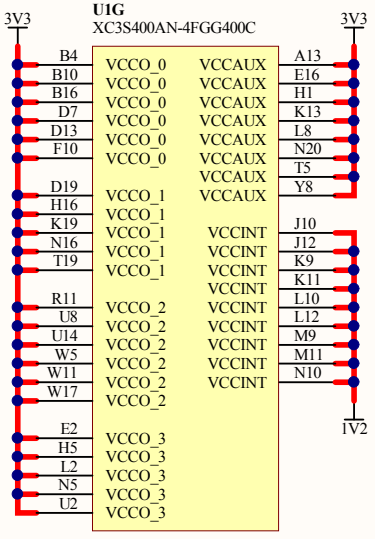

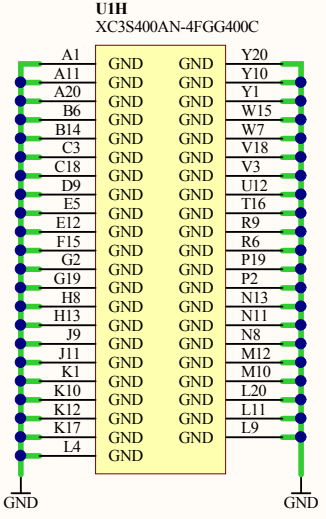

Sheet Title	*HOST FPGA Pwr and Programming*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:21 PM	Sheet 12 of 80	
File: HOST_FPGA_NonIO.SchDoc			

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USER/DB FPGA

JTAG

PROGRAM

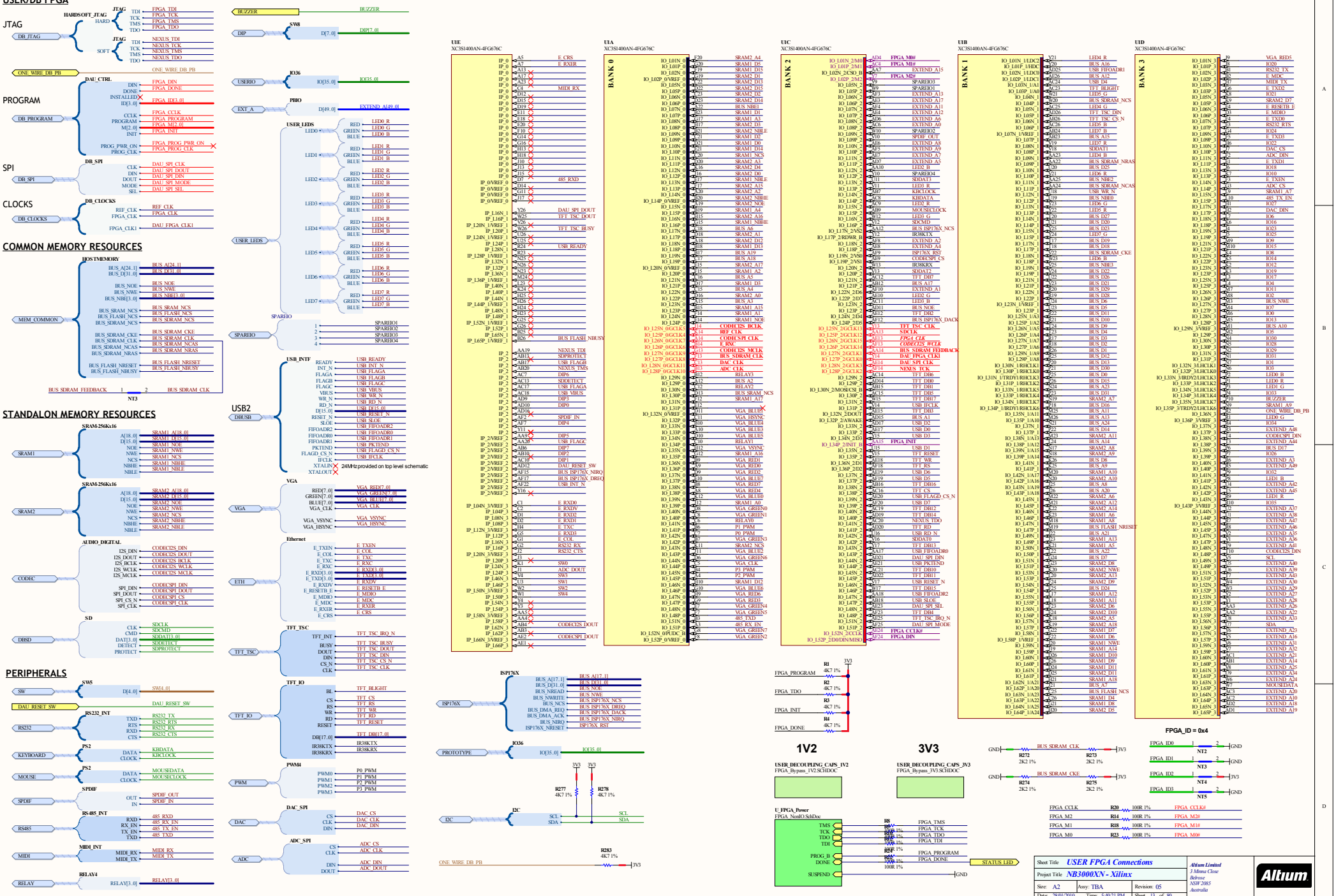
SPI

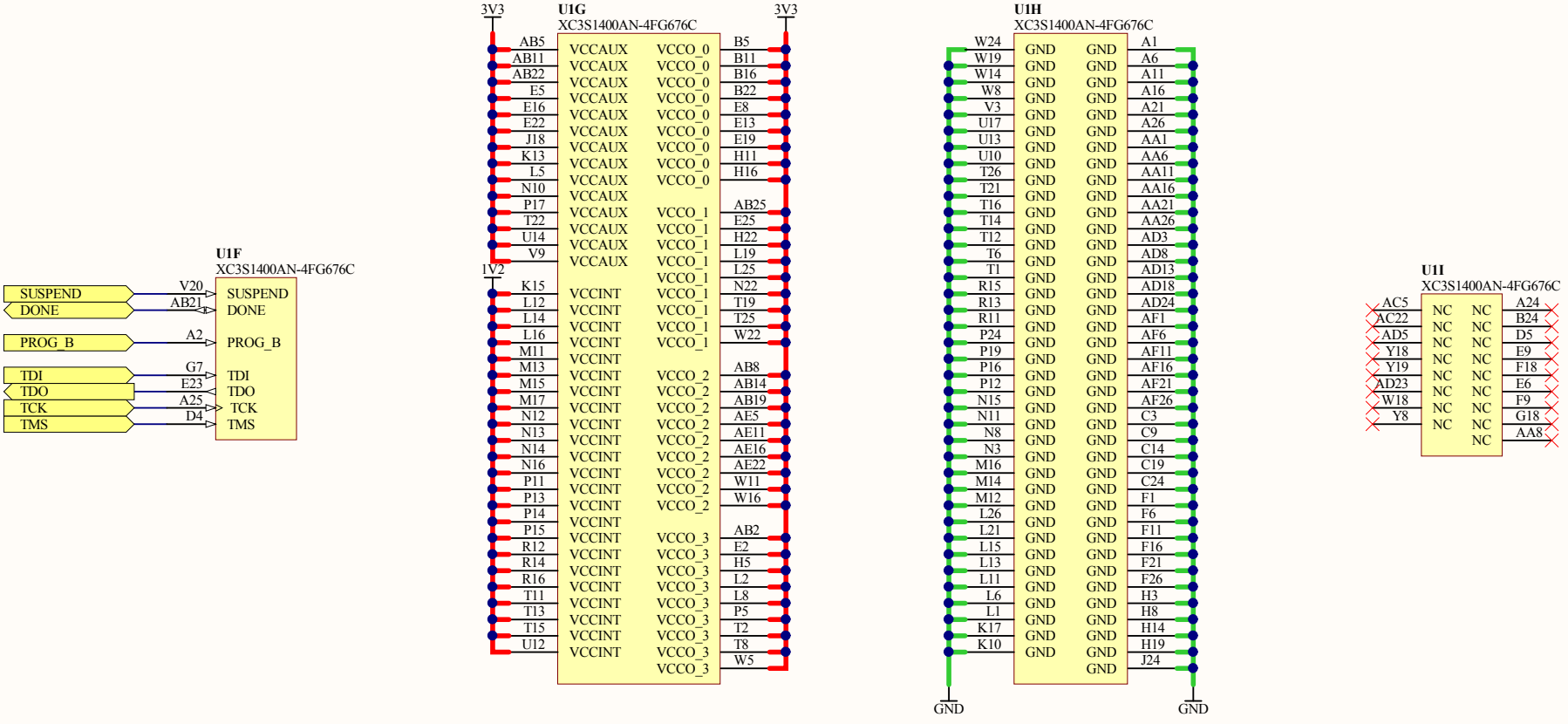
CLOCKS

COMMON MEMORY RESOURCES

STANDALON MEMORY RESOURCES

PERIPHERALS





Sheet Title	*USER FPGA Pwr and Programming*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 14 of 80	
File: FPGA_NonIO.SchDoc			

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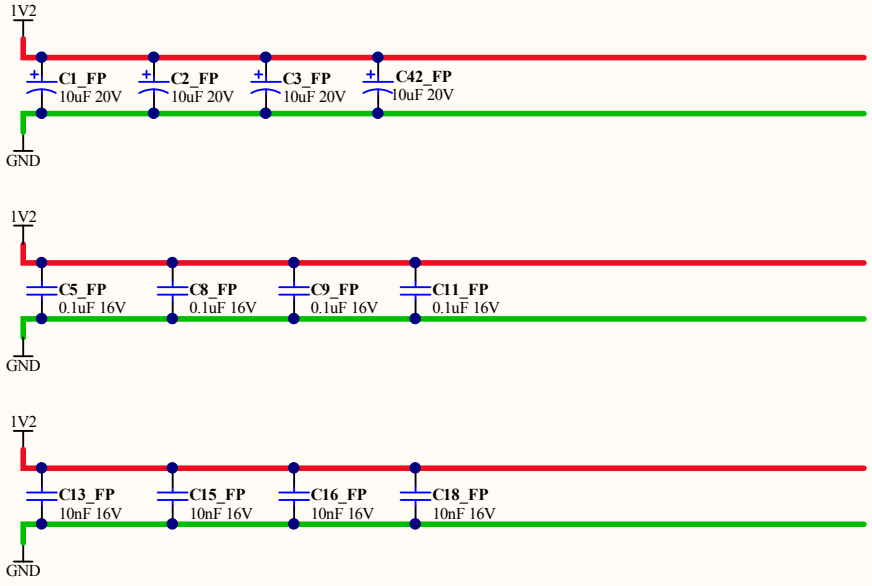

Sheet Title	*FPGA Bypass 1V2*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 15 of 80	
File: FPGA_Bypass_1V2.SCHDOC			

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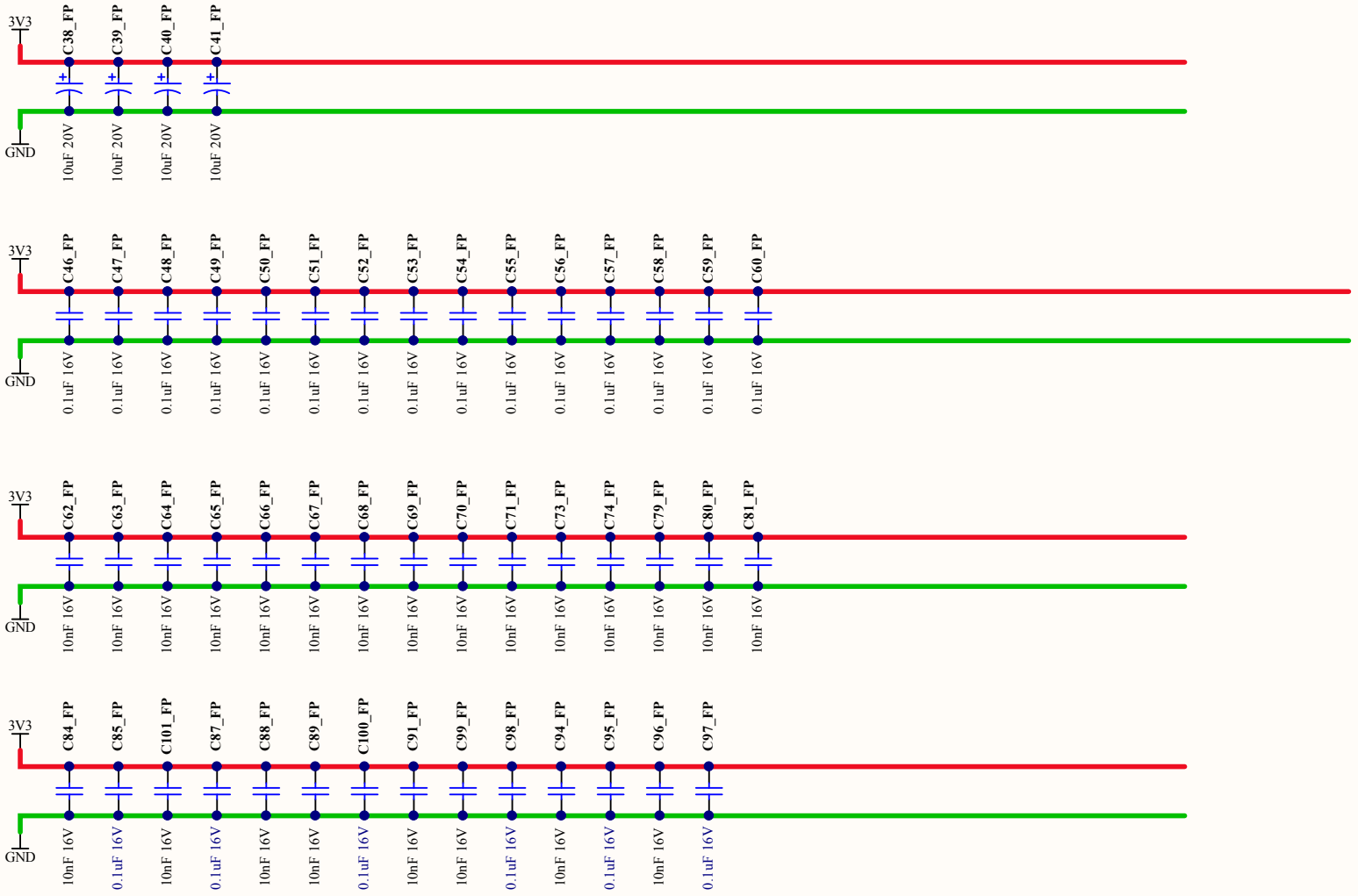

The FPGA bypass capacitors are physically grouped as 10nF and 100nF pairs on all major accessible power pins on the FPGA.

Sheet Title	*FPGA Bypass 3V3*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 16 of 80	
File: FPGA_Bypass_3V3.SCHDOC			

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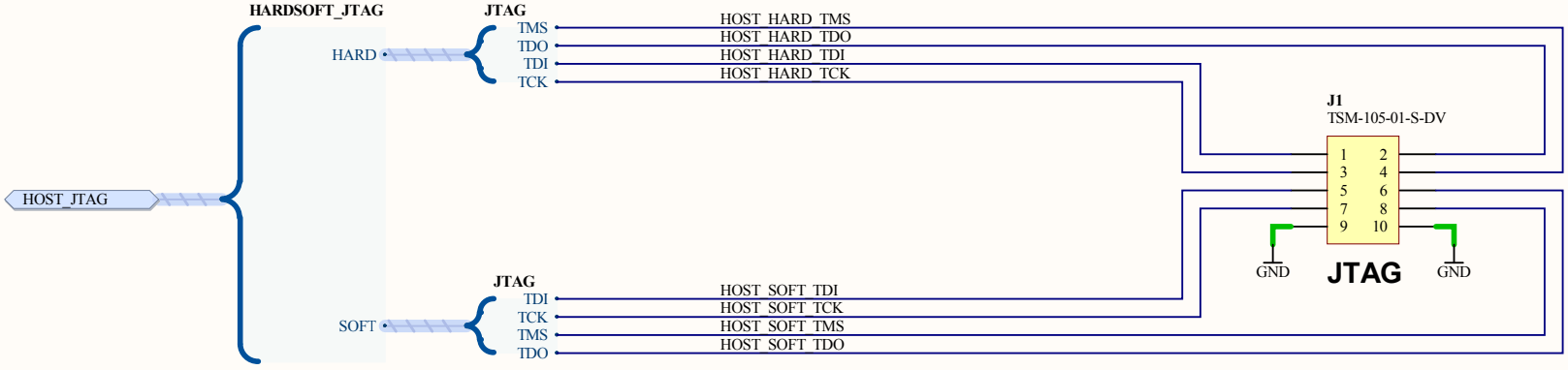

Sheet Title	*Local MCU Debug Connector*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 17 of 80	
File: HOST_JTAG.SchDoc			

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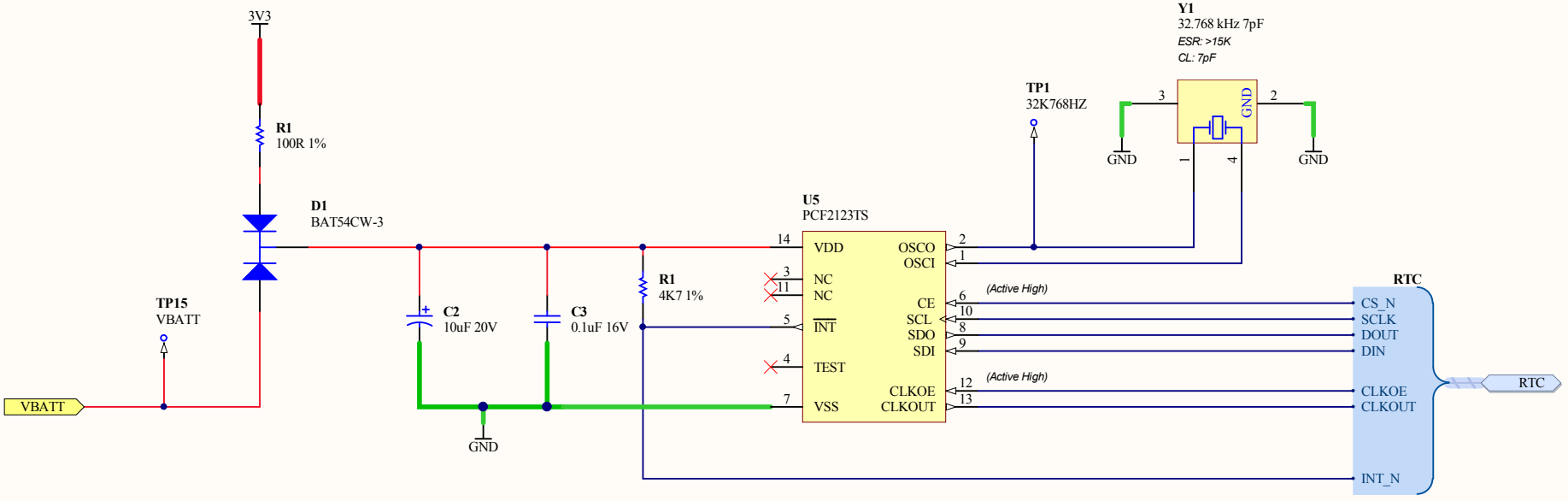

Sheet Title	*SPI Real Time Clock*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 18 of 80	
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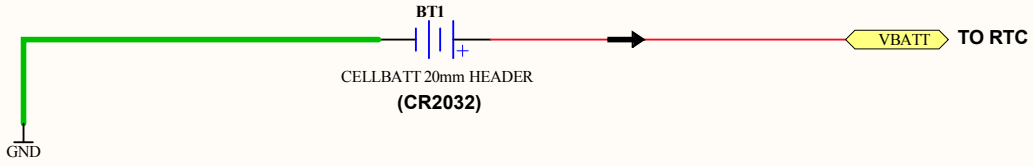

Sheet Title	*Lithium Battery Holder - CR2032*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 19 of 80	
File: CON_BATT_COIN.SchDoc			

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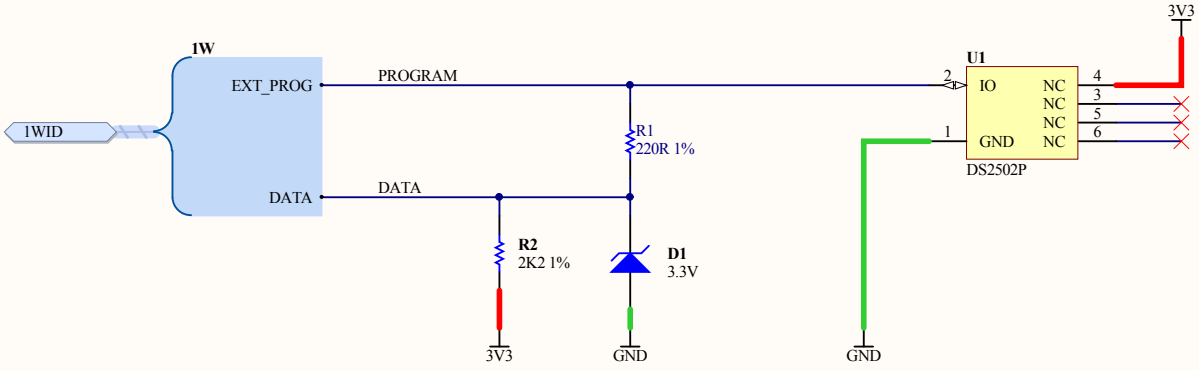

Sheet Title	***Protected 1-Wire EPROM***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 20 of 80	
File: 1WB_DS2502_ID.SchDoc			

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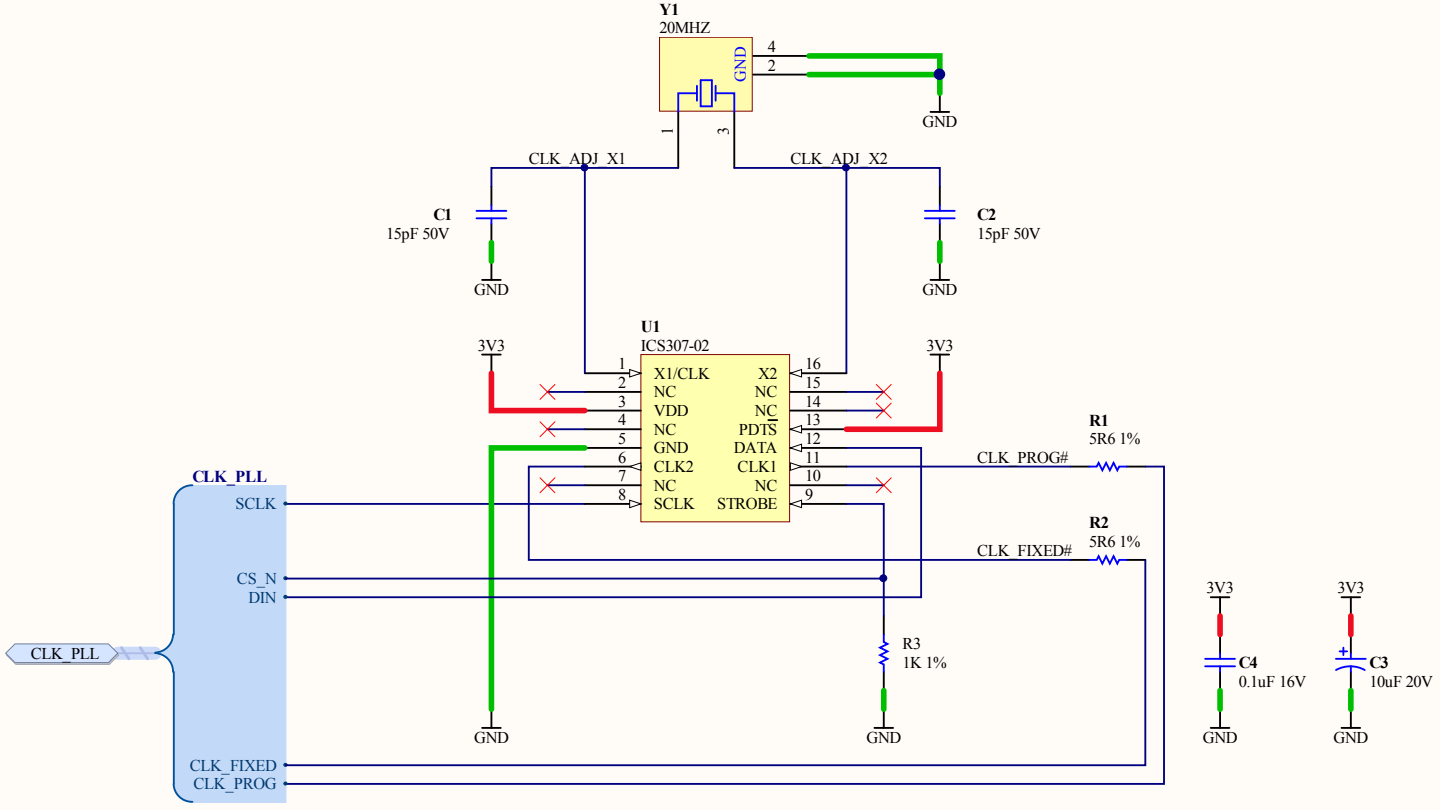

Sheet Title	***Programmable SPI Clock***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:22 PM	Sheet 21 of 80	
File: CLK_ICS307-02_PLL.SchDoc			

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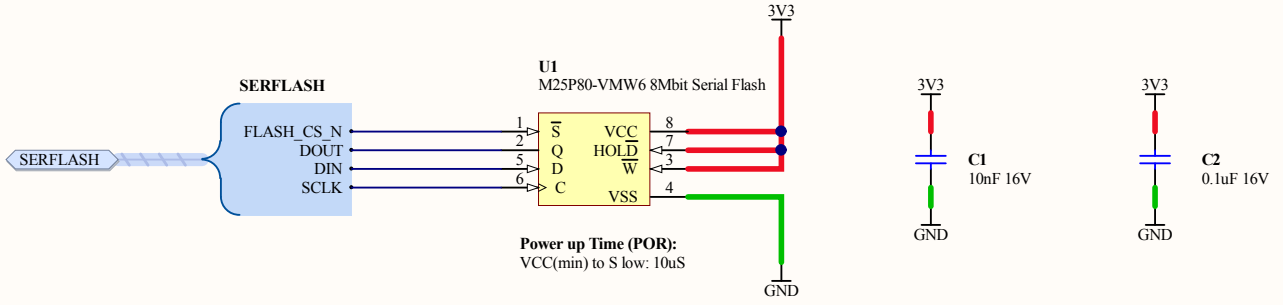

M25P80-VMW6 8Mbit Serial PROM *(75MHz)*

8,192,000 BITS

(ID=0x13)

Sheet Title	***Host - Dual Serial Flash Memory***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 22 of 80	
File: FLASH_M25PX0_SPI_8Mbit.SchDoc			

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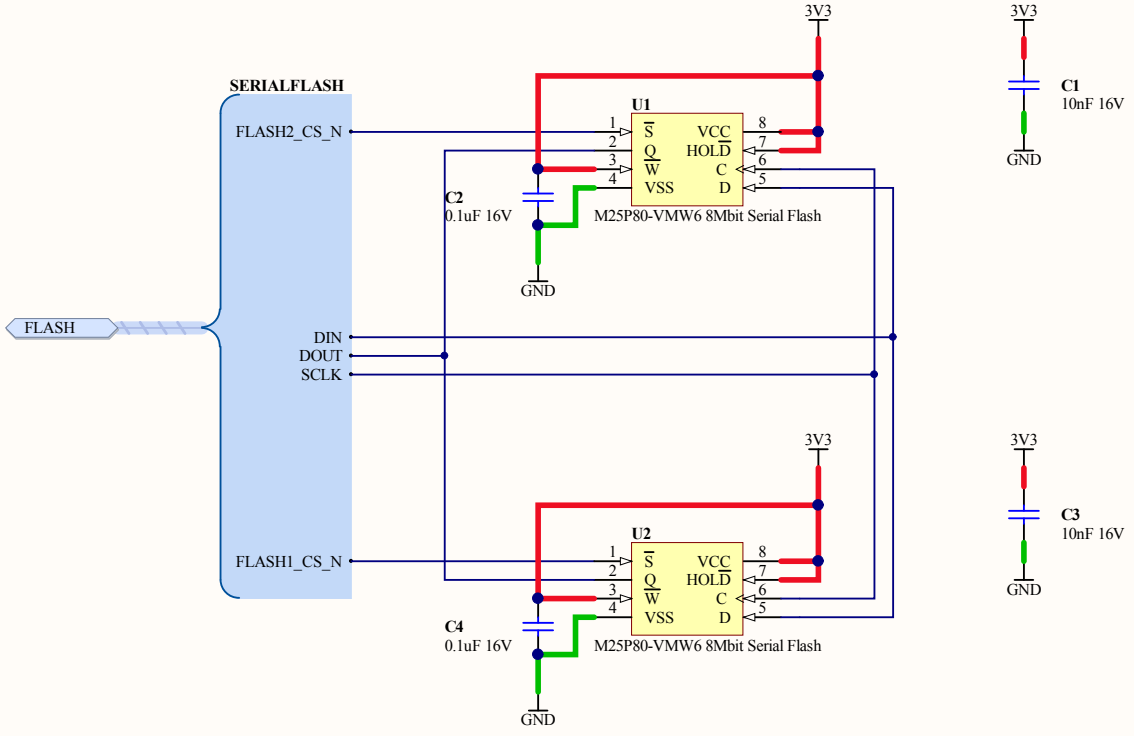

Sheet Title	*USER - Dual Serial Flash Memory*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 23 of 80	
File: FLASHSPI_M25PX0.SchDoc			

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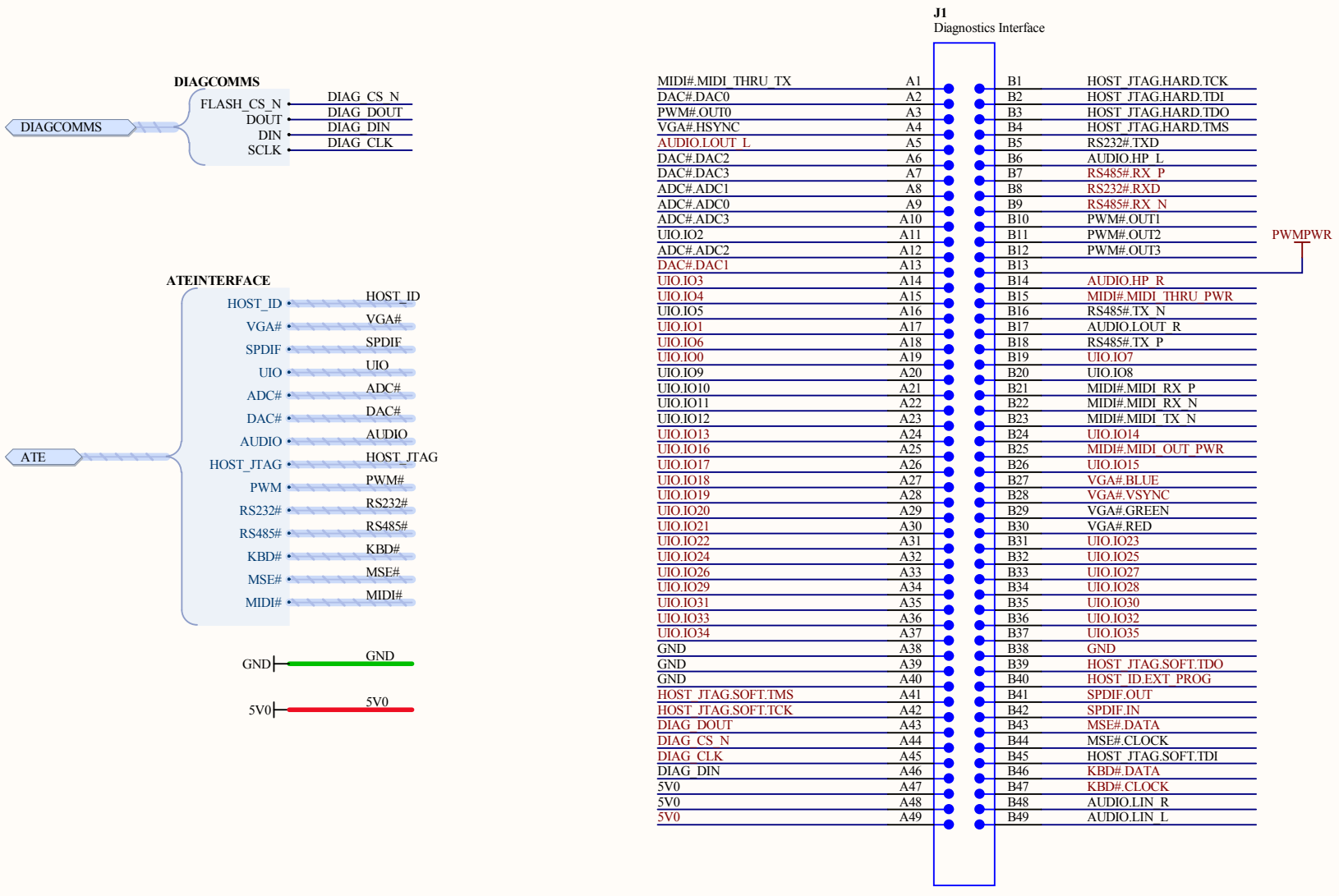
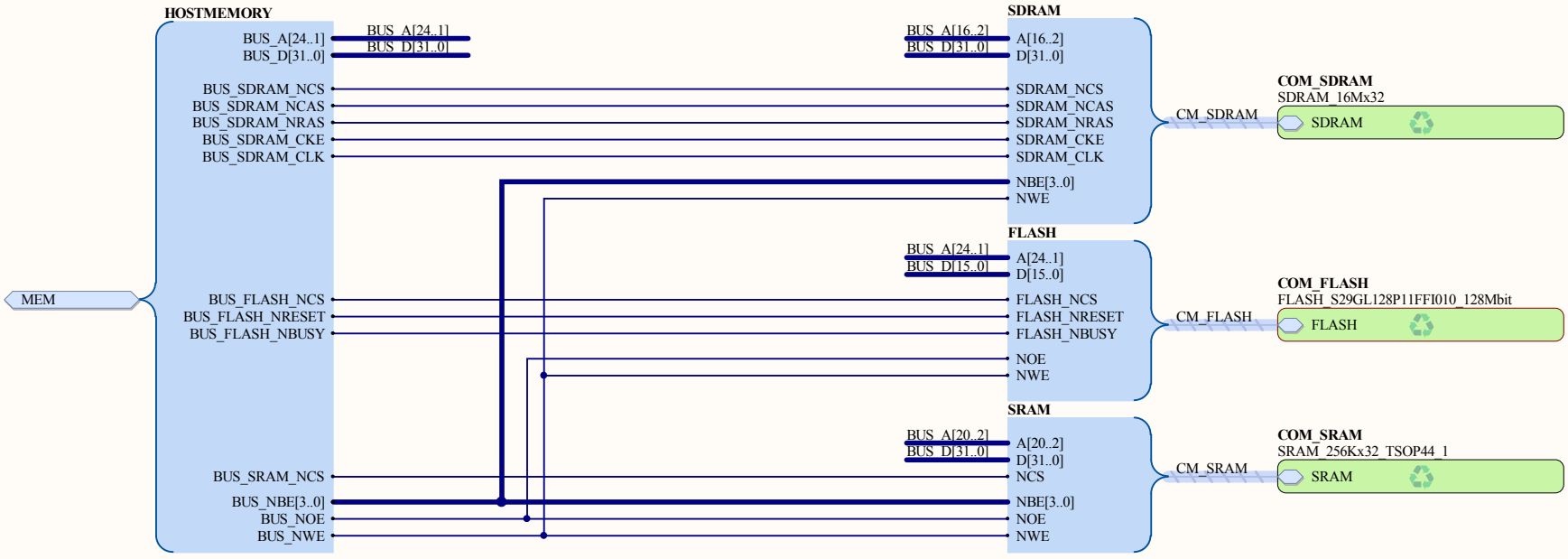


Title	*ATE Interface Connector*		*Altium Limited.* *3 Minna Close* *Belrose* *NSW 2085* *AUSTRALIA*
Size: A4	Number:	Revision: 05	
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 24 of 80	
File: C:\Program Files\Altium Designer Summer 09 - Beta\Examples\Reference Designs\NanoBoard-NB3000XN\Dependencies\Device She			



Common-Bus Memory Block

256K x 32-bit SRAM (1 MByte)
16M x 32-Bit SDRAM (64 MByte)
8M x 16-Bit Flash (16 MByte)

Sheet Title	*Common-Bus Memory Block*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 25 of 80	
File: CommonMemory.SchDoc			

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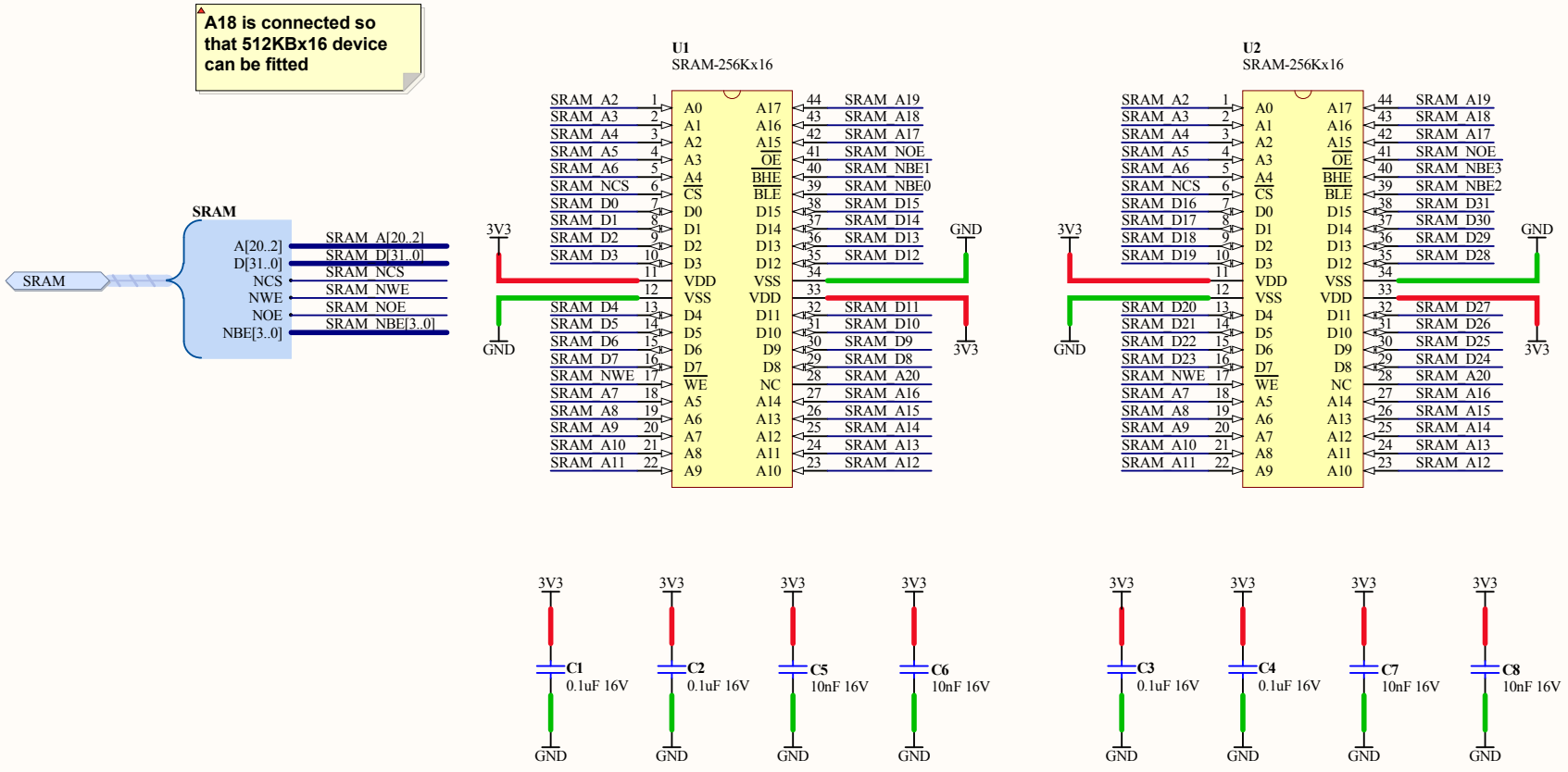

Sheet Title	*256K x 32 SRAM - TSOP44 x 2*	
Project Title	*NB3000XN - Xilinx*	
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 26 of 80
File: SRAM_256Kx32_TSOP44_1.SchDoc		

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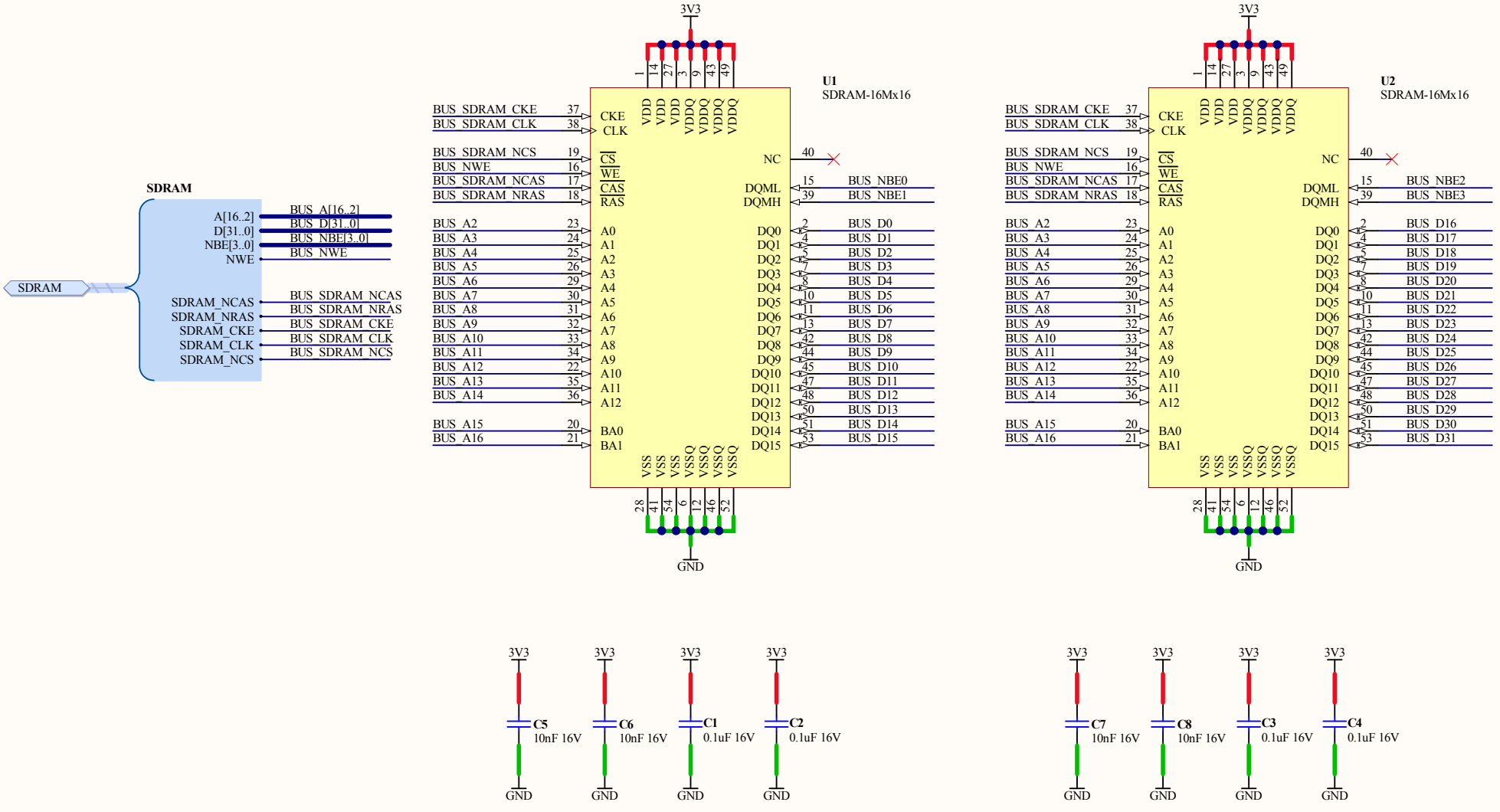

Sheet Title	*16M x 32 SDRAM TSOP54 x 2*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 27 of 80	
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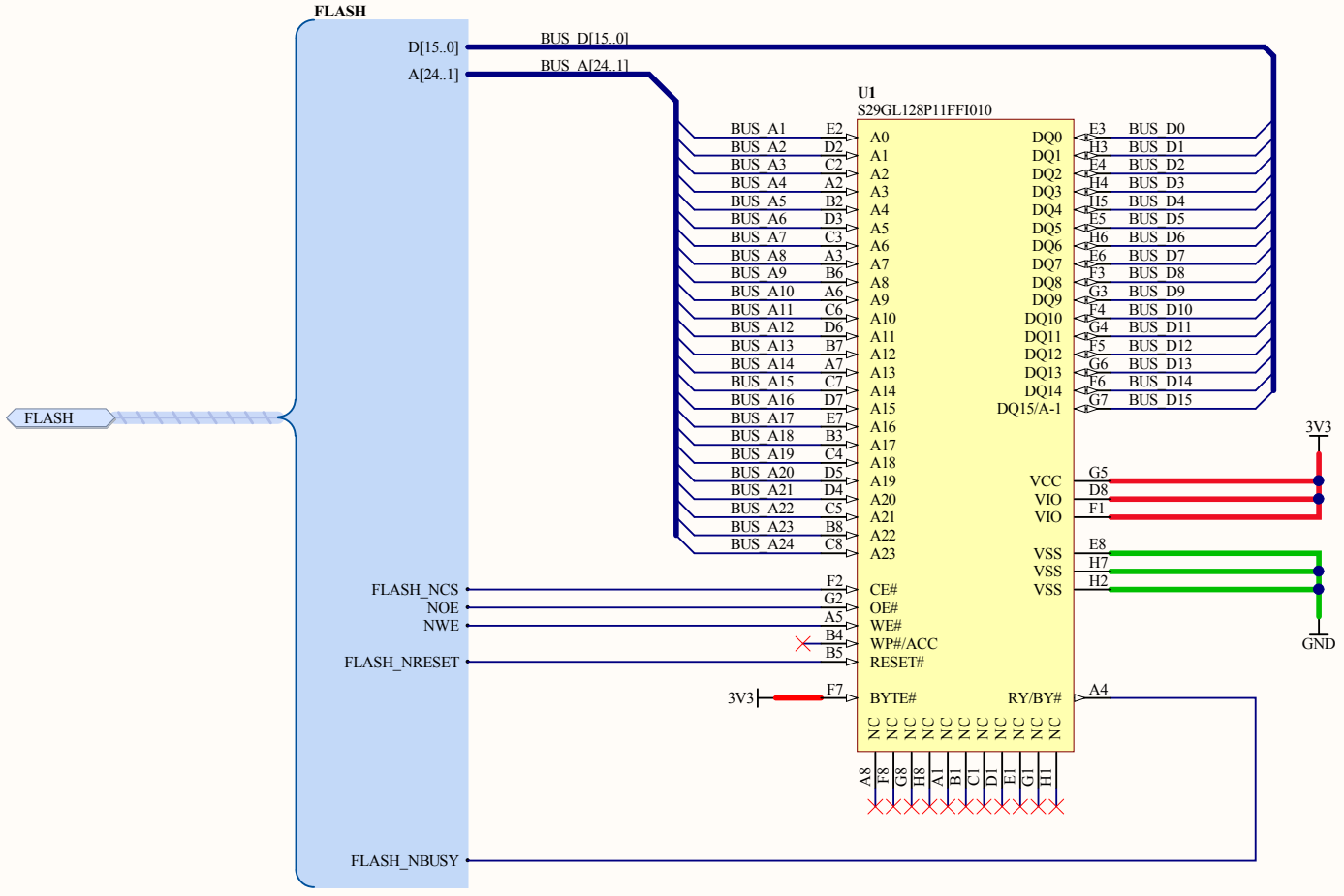

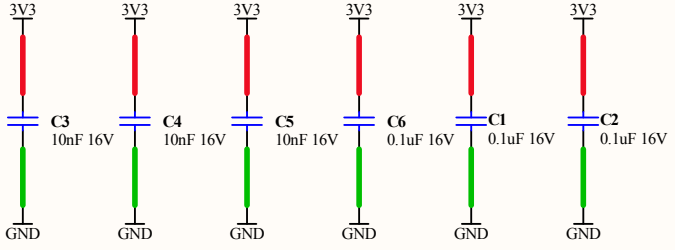

Sheet Title	*128M-bit Flash Memory (BGA)*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 28 of 80	
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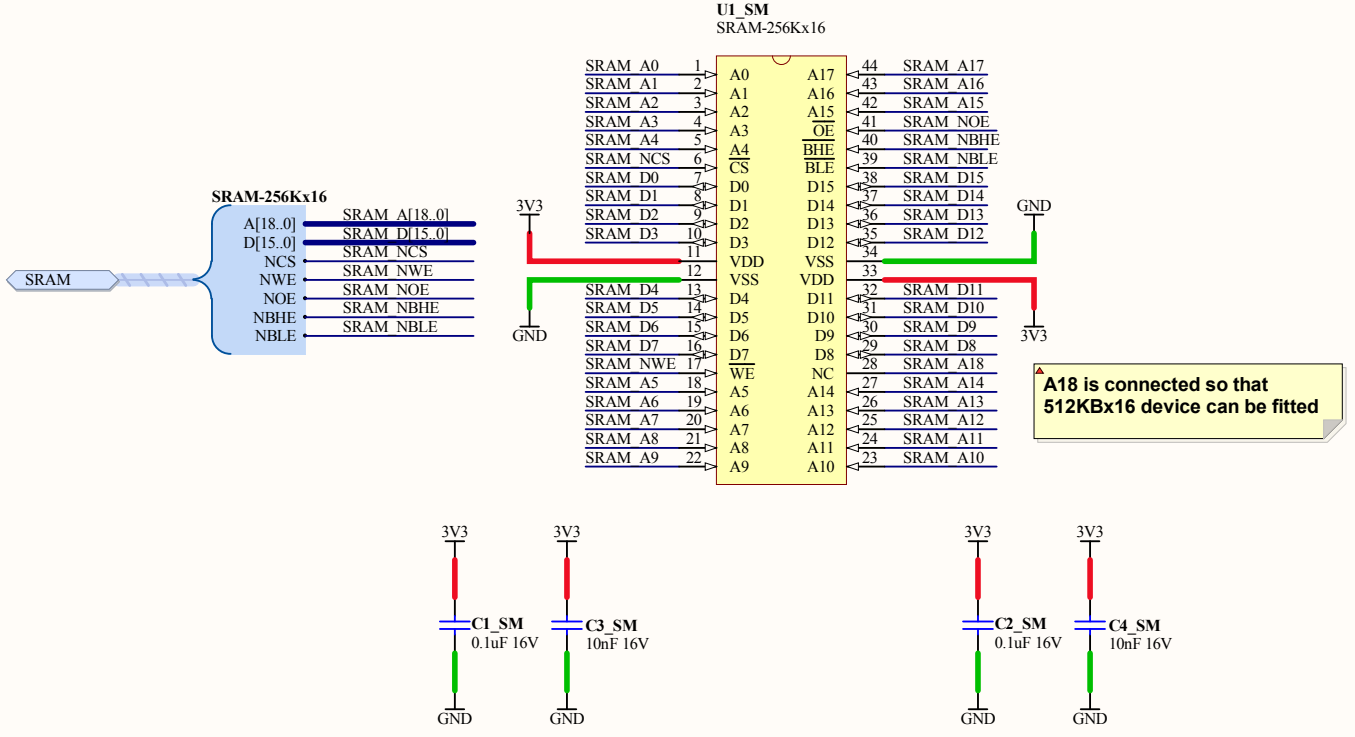

Sheet Title	*256K x 16-Bit SRAM*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:23 PM	Sheet 29 of 80	
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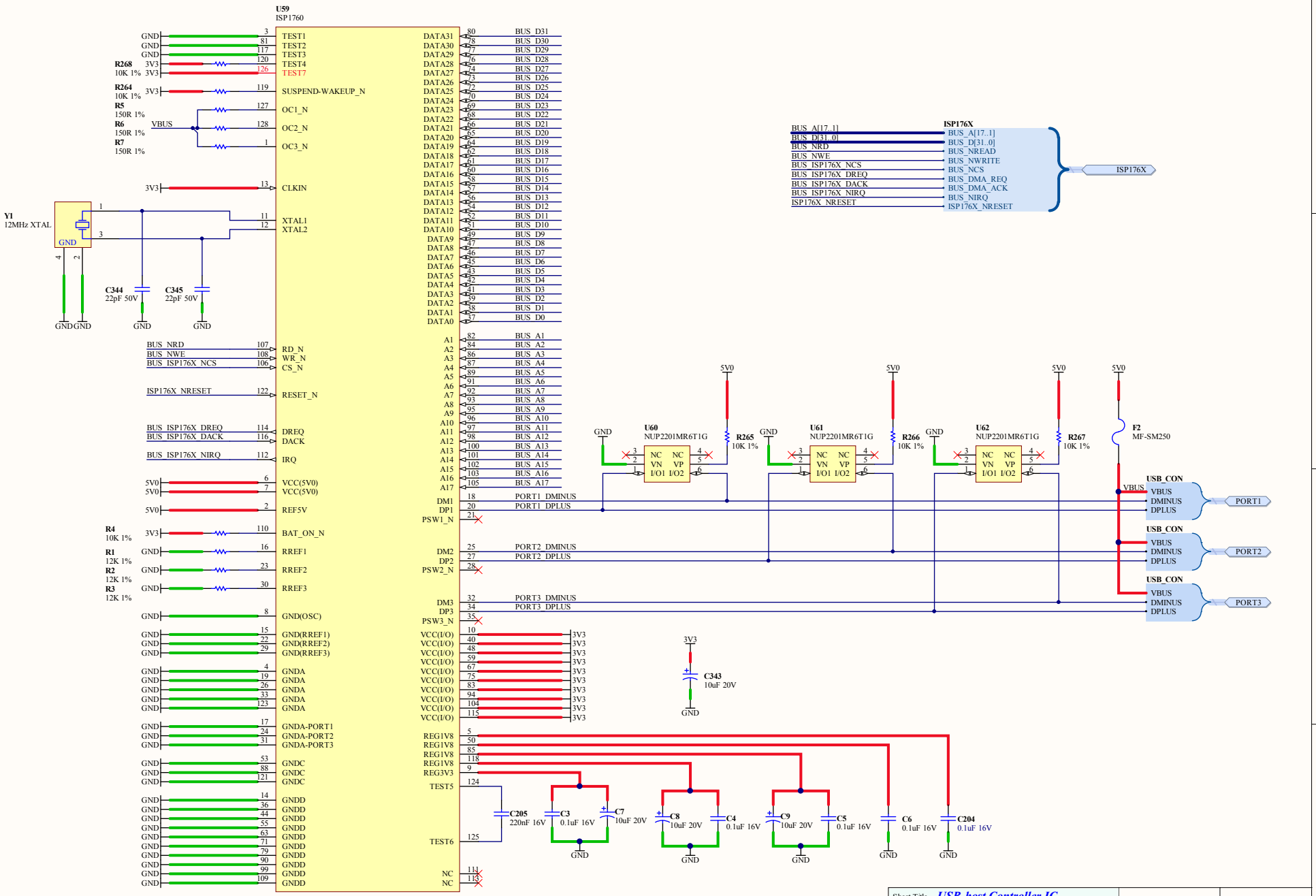

Sheet Title	*USB-host Controller IC*		
Project Title	*NB3000XN - Xilinx*		
Size: A3	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:24 PM	Sheet 30 of 80	
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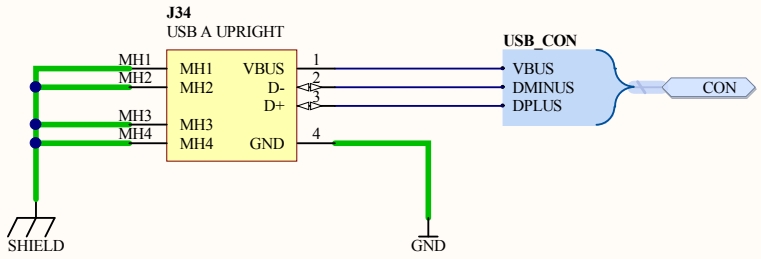

Sheet Title	*USBA RA Upright Connector*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:24 PM	Sheet 31 of 80	
File: CON_USBA_RA_UPRIGHT.SchDoc			

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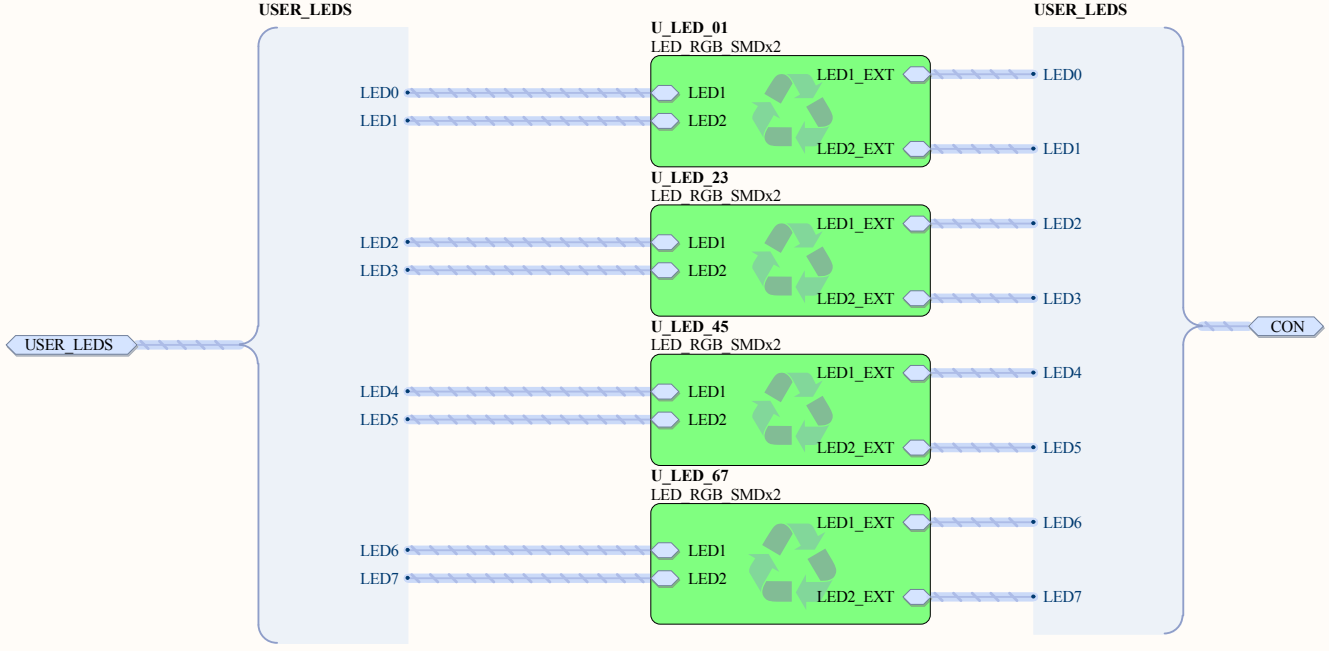

Sheet Title	*Visual Indicators*	
Project Title	*NB3000XN - Xilinx*	
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010	Time: 5:40:24 PM	Sheet 32 of 80
File: LED_RGB_SMDx8.SCHDOC		

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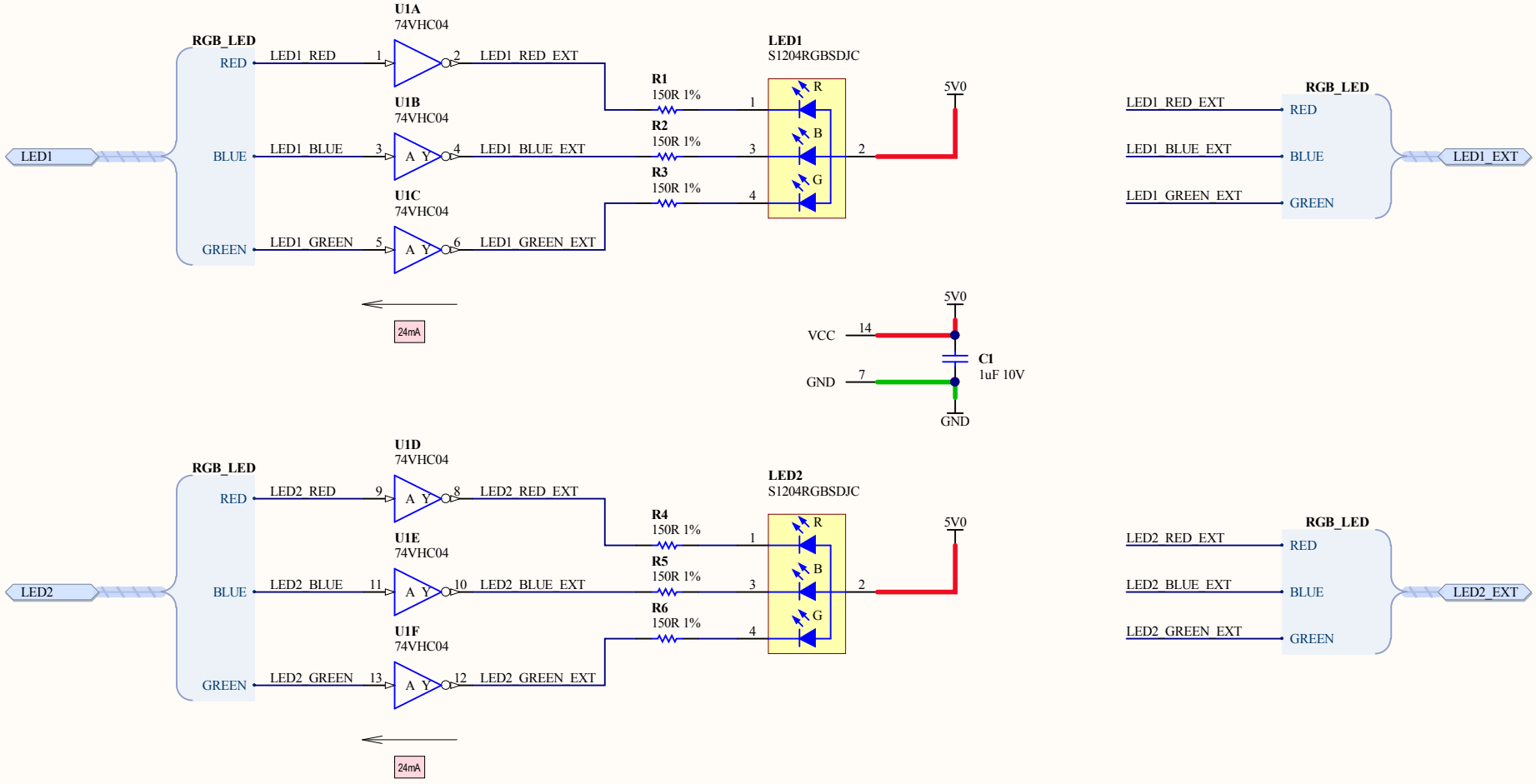

Sheet Title	*Visual Indicators*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:24 PM	Sheet 33 of 80	
File: LED_RGB_SMDx2.SCHDOC			

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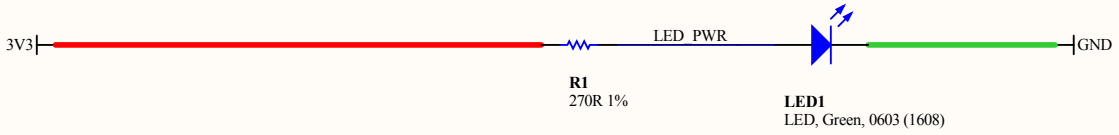
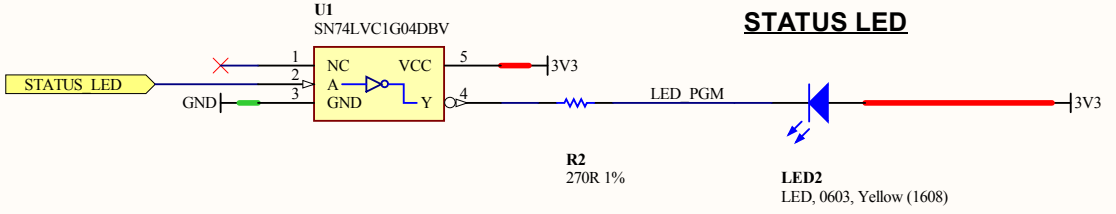
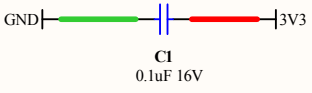
POWER LED



STATUS LED





Sheet Title	*User FPGA Status LEDs*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:24 PM	Sheet 34 of 80	
File: DB_LEDS_0603.SchDoc			

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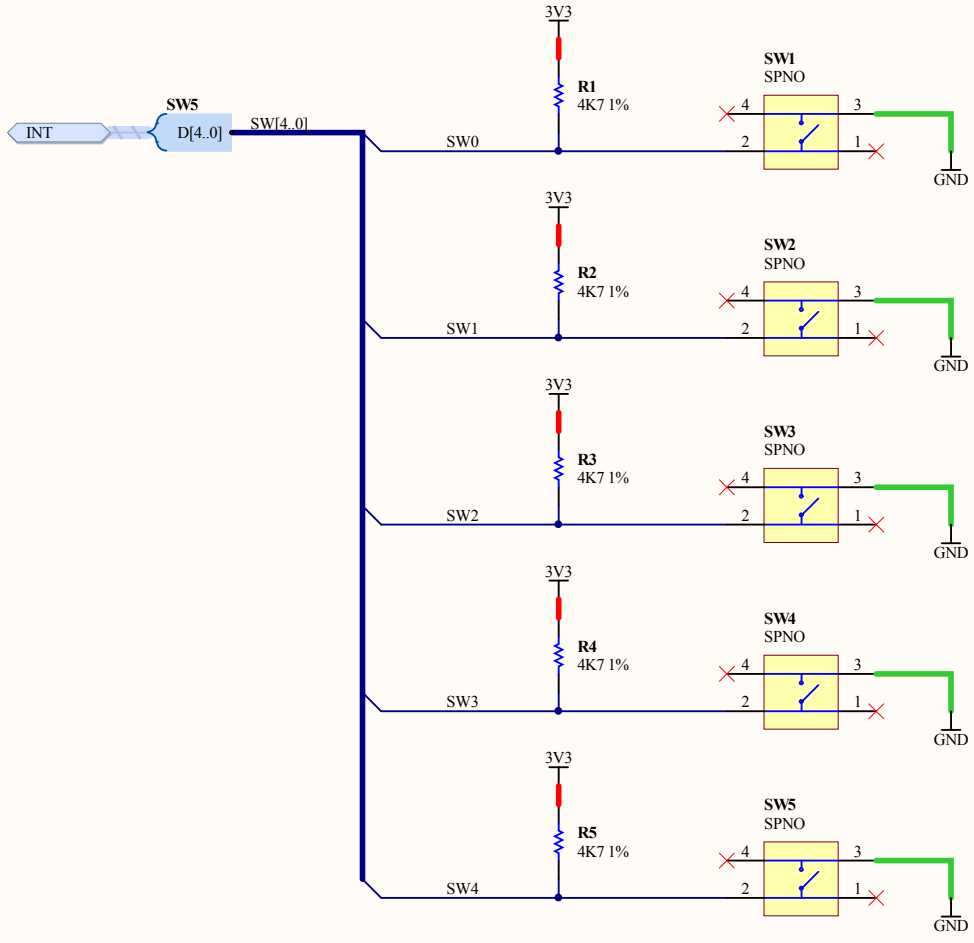

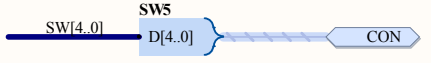

Sheet Title	***PDA-Style 5 x SPNO Switch***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:24 PM	Sheet 35 of 80	
File: SW_PB_SPNOx5_SMD.SCHDOC			

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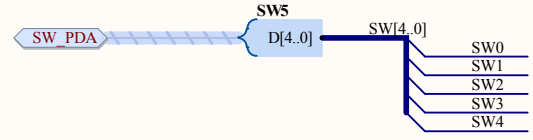

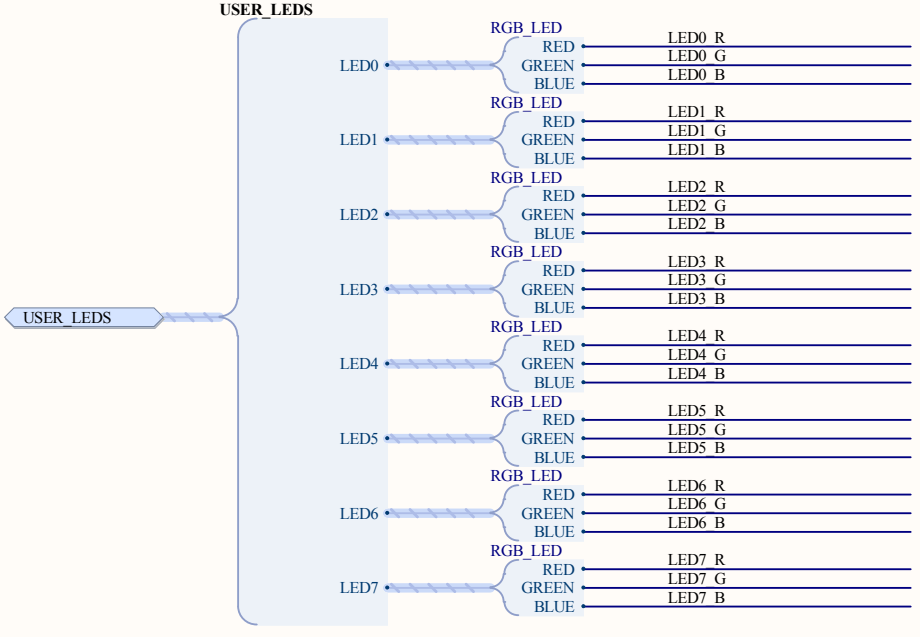

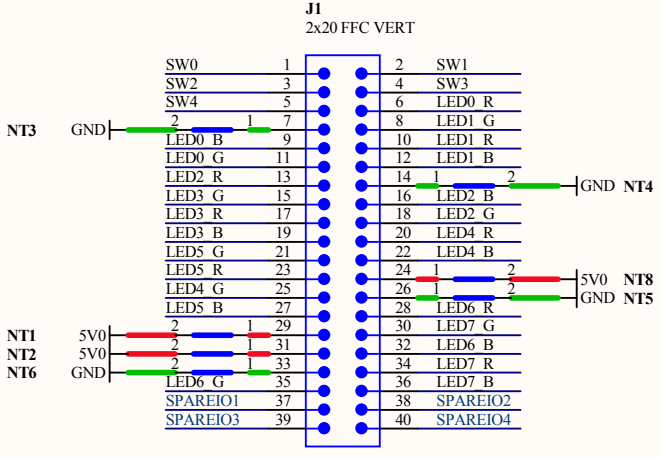

Sheet Title	*LED and Button Ext. Connector*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:24 PM	Sheet 36 of 80	
File: CON_NB3000_LEDKB.SCHDOC			

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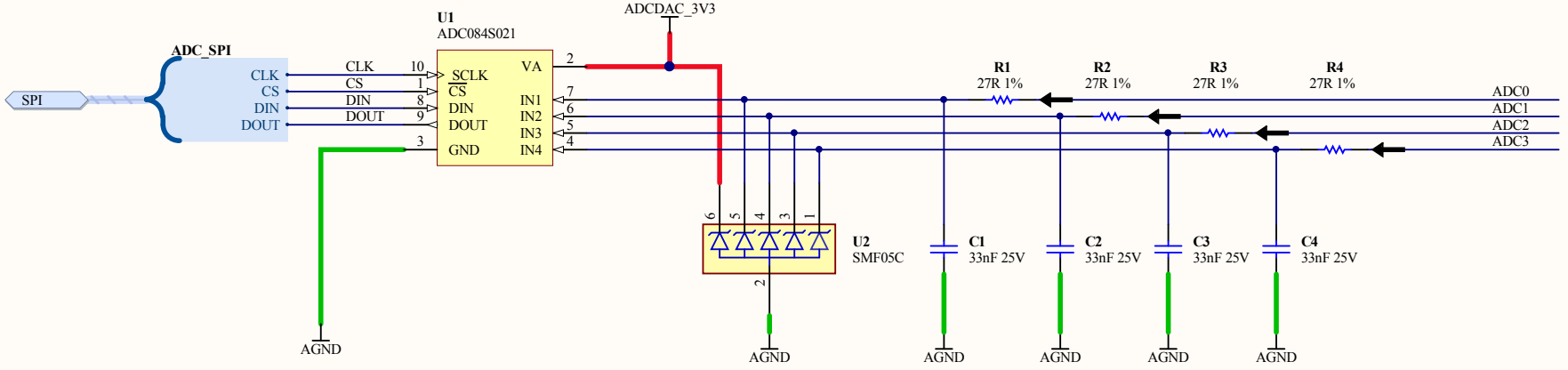

ADC maximum sample rate:

8 bit @ 200Ksps

Maximum sample rate (nyquist) : 100kHz

0.012890625v = 1 bit (3V3 ref) resolution

Low Pass Input filter Calculations:

R = 27 Ohms
C = 33nF (0.033uF)

$$f_c = \frac{1}{2\pi RC}\ Hz = \frac{1}{6.38 \times 27 \times 33^{-9}}$$

= 178715.6777

= Corner frequency rolloff (Knee) of ~ 178KHz

Sheet Title: ***ADC084S021 8-Bit ADC IC***		
Project Title: ***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010 Time: 5:40:24 PM		Sheet 37 of 80
File: ADC_ADC084S021_SPI.SchDoc		

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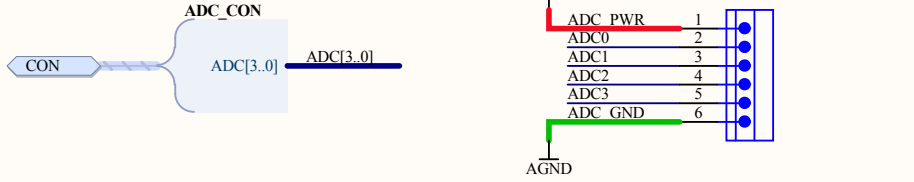

Sheet Title	***Screw Header For ADC***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 38 of 80	
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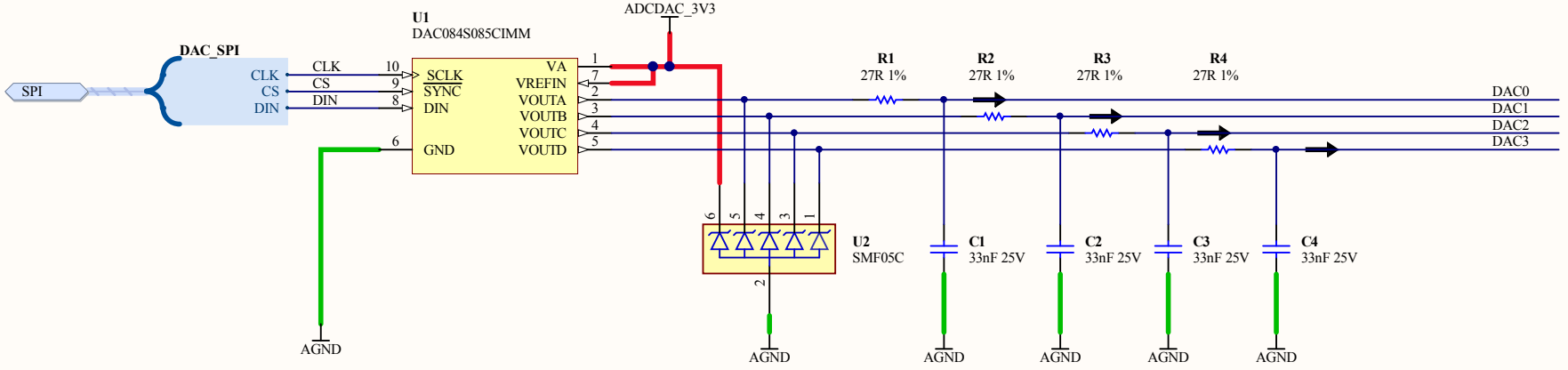

Sheet Title	*DAC084S085 8-bit DAC IC*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 39 of 80	
File: DAC_DAC084S085_SPI.SchDoc			

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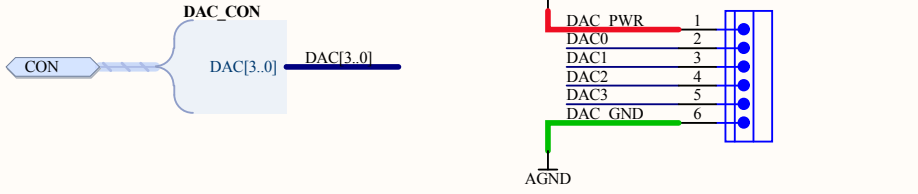

Sheet Title	***Screw Header For DAC***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 40 of 80	
File: CON_DACx4_KMRJIO3_5MM_6WAY.SchDoc			

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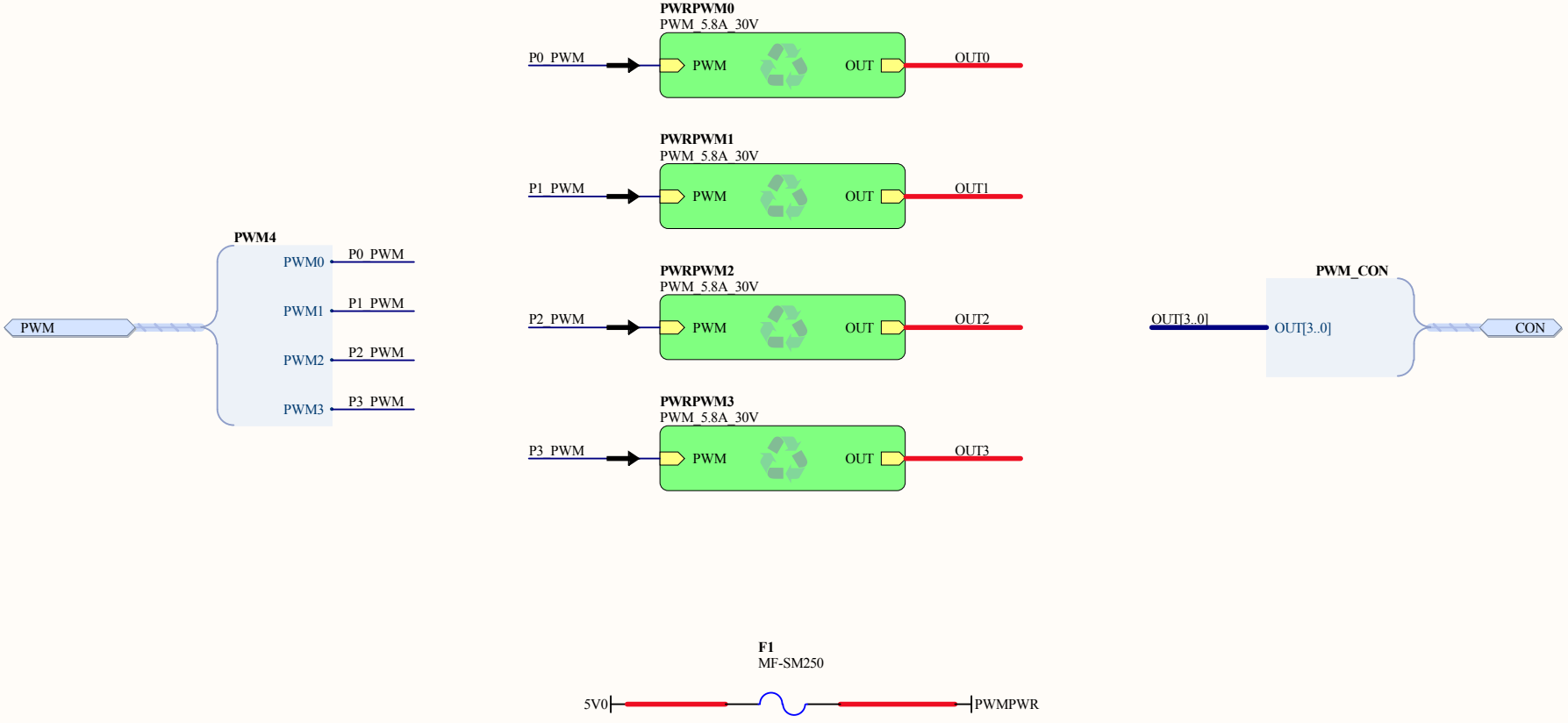

Sheet Title	***PWM x 4***	
Project Title	***NB3000XN - Xilinx***	
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 41 of 80
File: PWM_5.8A_30V_X4.SchDoc		

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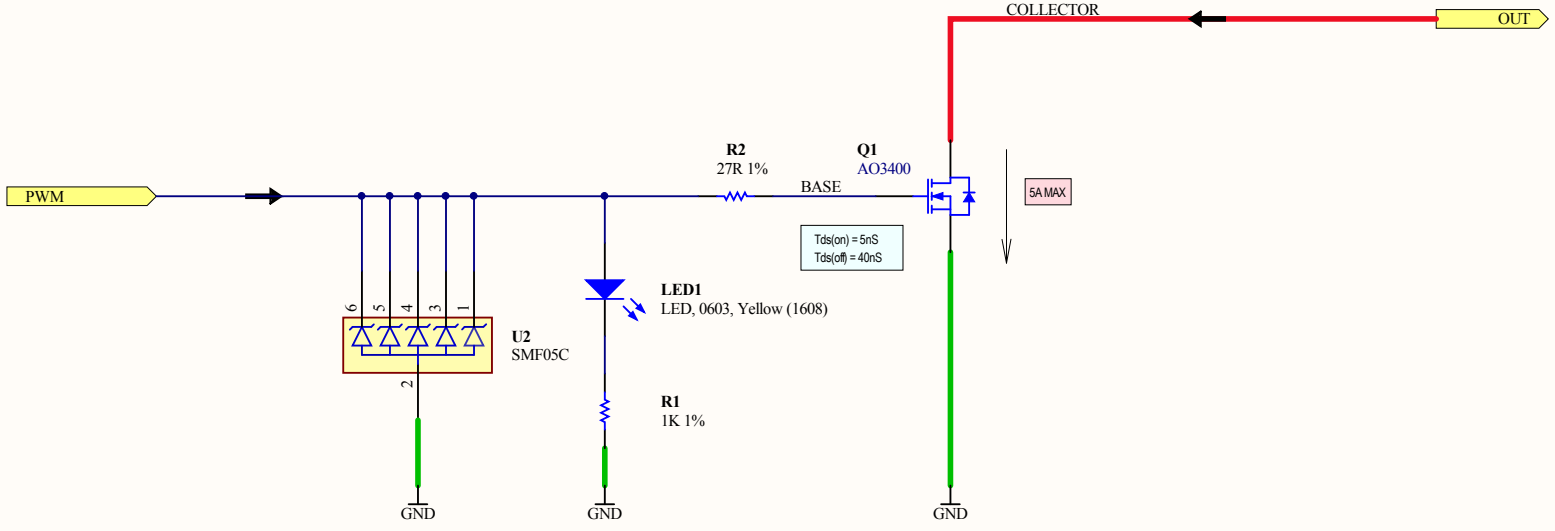

Sheet Title	***PWM 30V/4A***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 42 of 80	
File: PWM_5.8A_30V.SchDoc			

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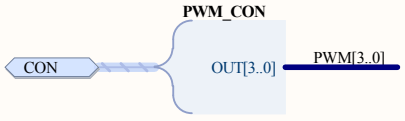

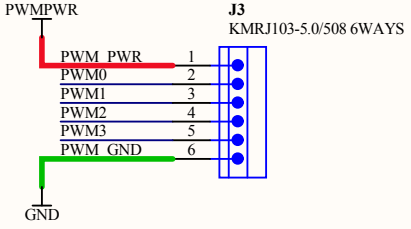

Sheet Title	***Screw Header For Power PWM***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 43 of 80	
File: CON_PWMx4_KMRJIO3_5MM_6WAY.SchDoc			

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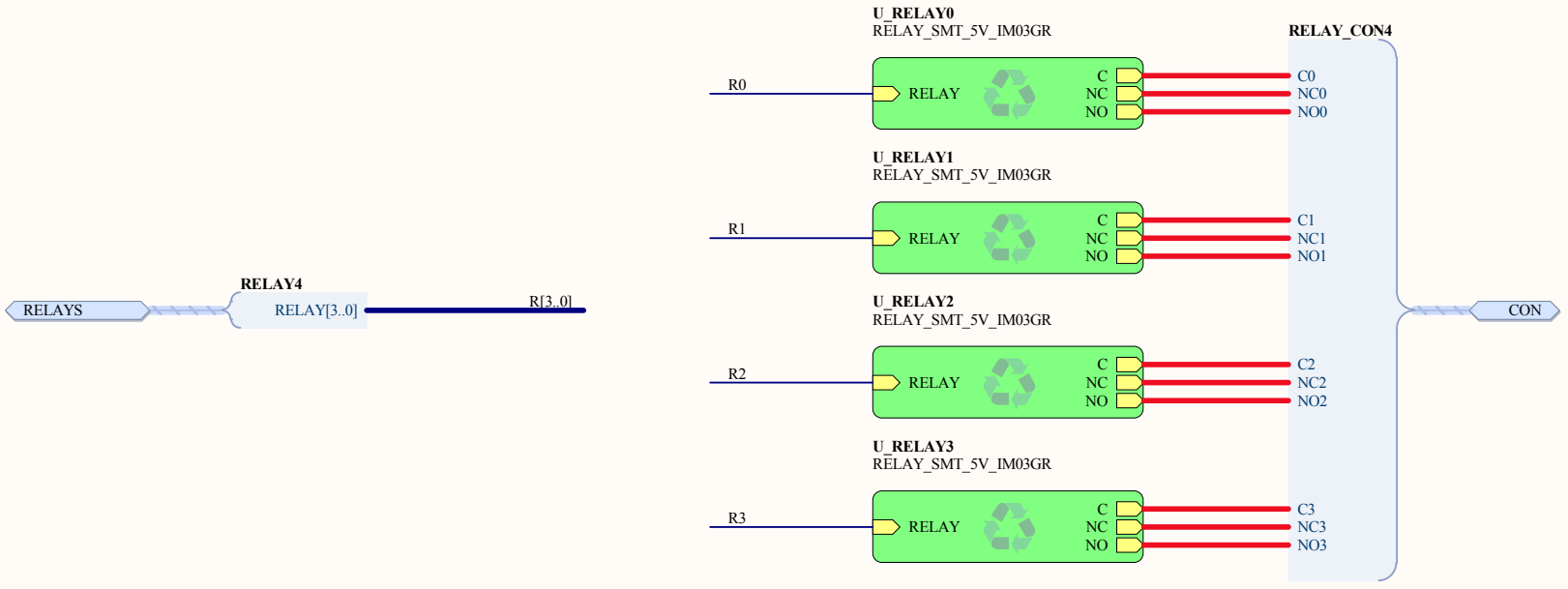

Sheet Title	***Power Control x4***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 44 of 80	
File: RELAY_X4_IM03GR.SchDoc			

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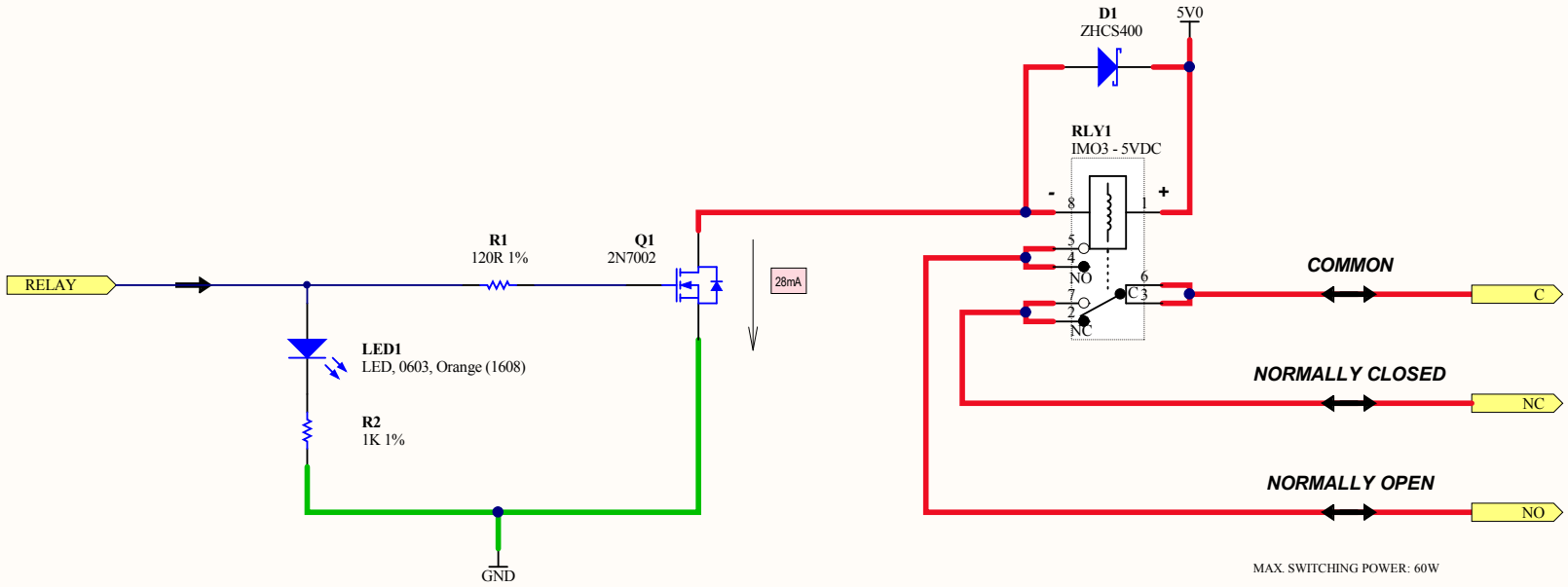

Sheet Title	***Power Control***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:25 PM	Sheet 45 of 80	
File: RELAY_SMT_5V_IM03GR.SchDoc			

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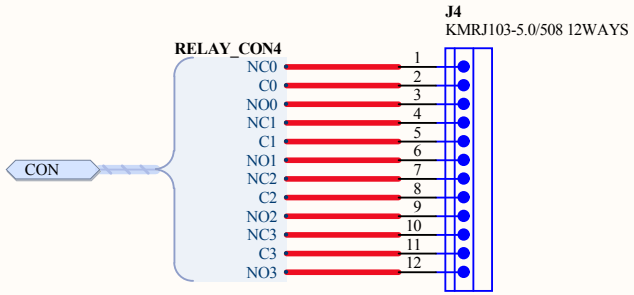

Sheet Title	***Screw Header For Relays***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:26 PM	Sheet 46 of 80	
File: CON_RELAYx4_KMRJIO3_5MM_12WAY.SchDoc			

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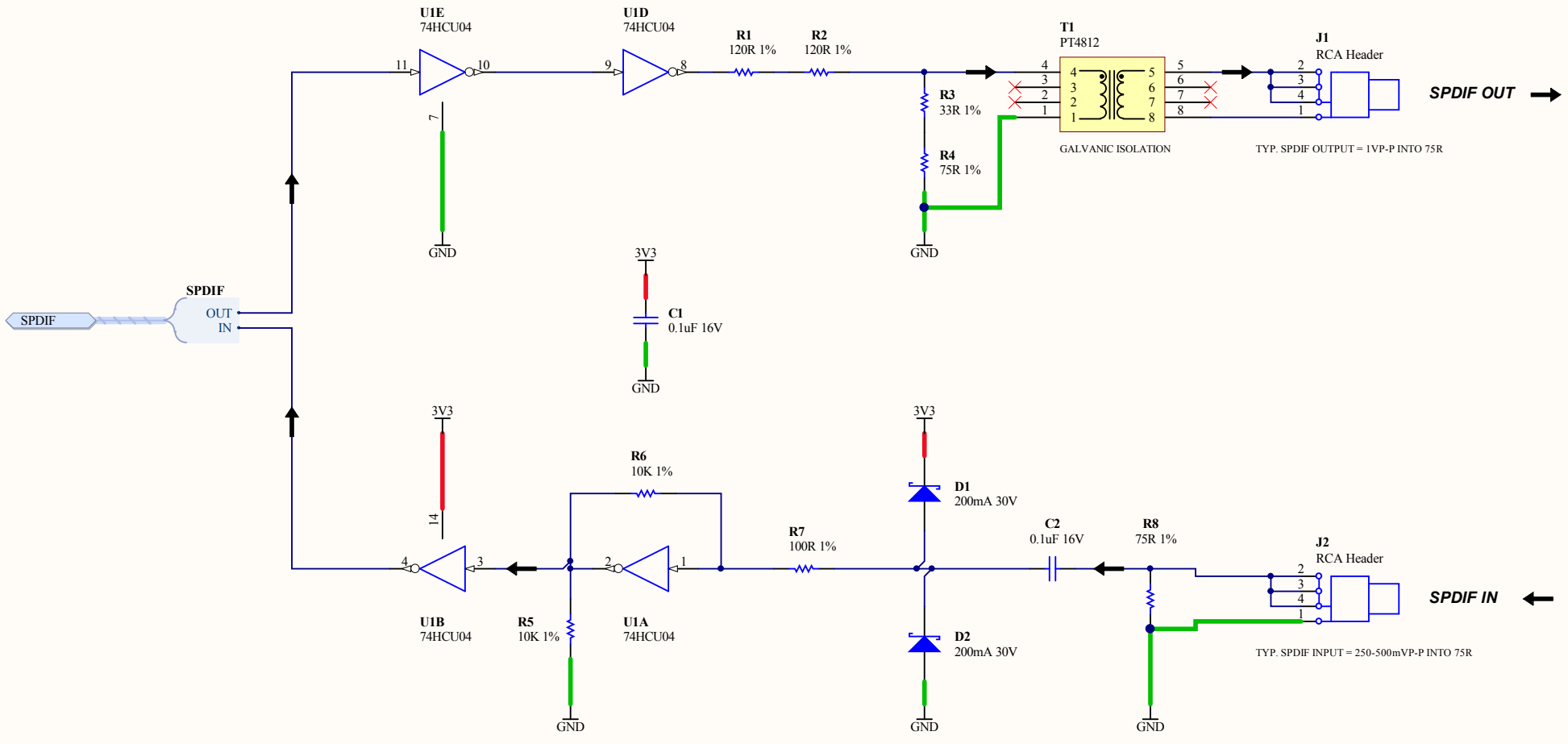

NOTE:
INVERTER MUST BE UNBUFFERED (U TYPE)

U1F
74HCU04

U1C
74HCU04

Sheet Title	*S/PDIF RCA IN/OUT*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:26 PM	Sheet 47 of 80	
File: CON_SPDIF_INOUT_A.SchDoc			

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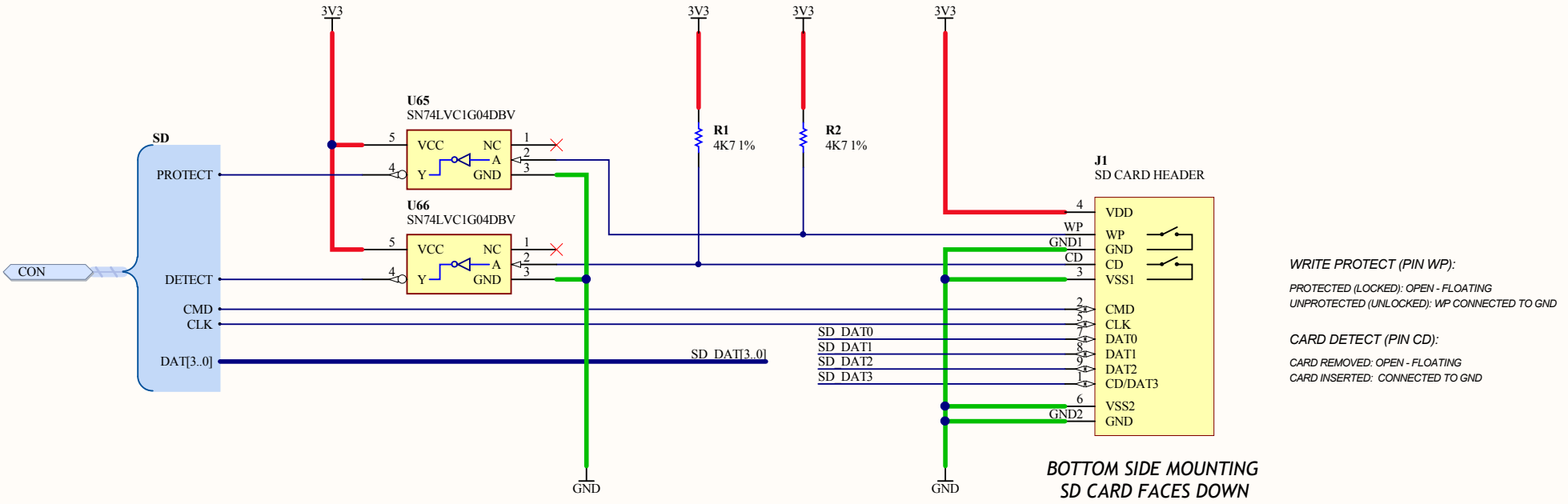

WRITE PROTECT (PIN WP):

PROTECTED (LOCKED): OPEN - FLOATING
UNPROTECTED (UNLOCKED): WP CONNECTED TO GND

CARD DETECT (PIN CD):

CARD REMOVED: OPEN - FLOATING
CARD INSERTED: CONNECTED TO GND

BOTTOM SIDE MOUNTING
SD CARD FACES DOWN

Sheet Title	***SD-CARD***	
Project Title	***NB3000XN - Xilinx***	
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010	Time: 5:40:26 PM	Sheet 48 of 80
File: CON_SD_KSDC012551.SchDoc		

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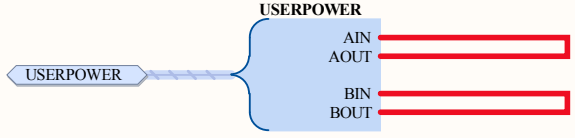

USER HEADER
POWER LOOPBACK

Sheet Title	***USER HEADER POWER***	
Project Title	***NB3000XN - Xilinx***	
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010	Time: 5:40:26 PM	Sheet 49 of 80
File: USERPWR.SchDoc		

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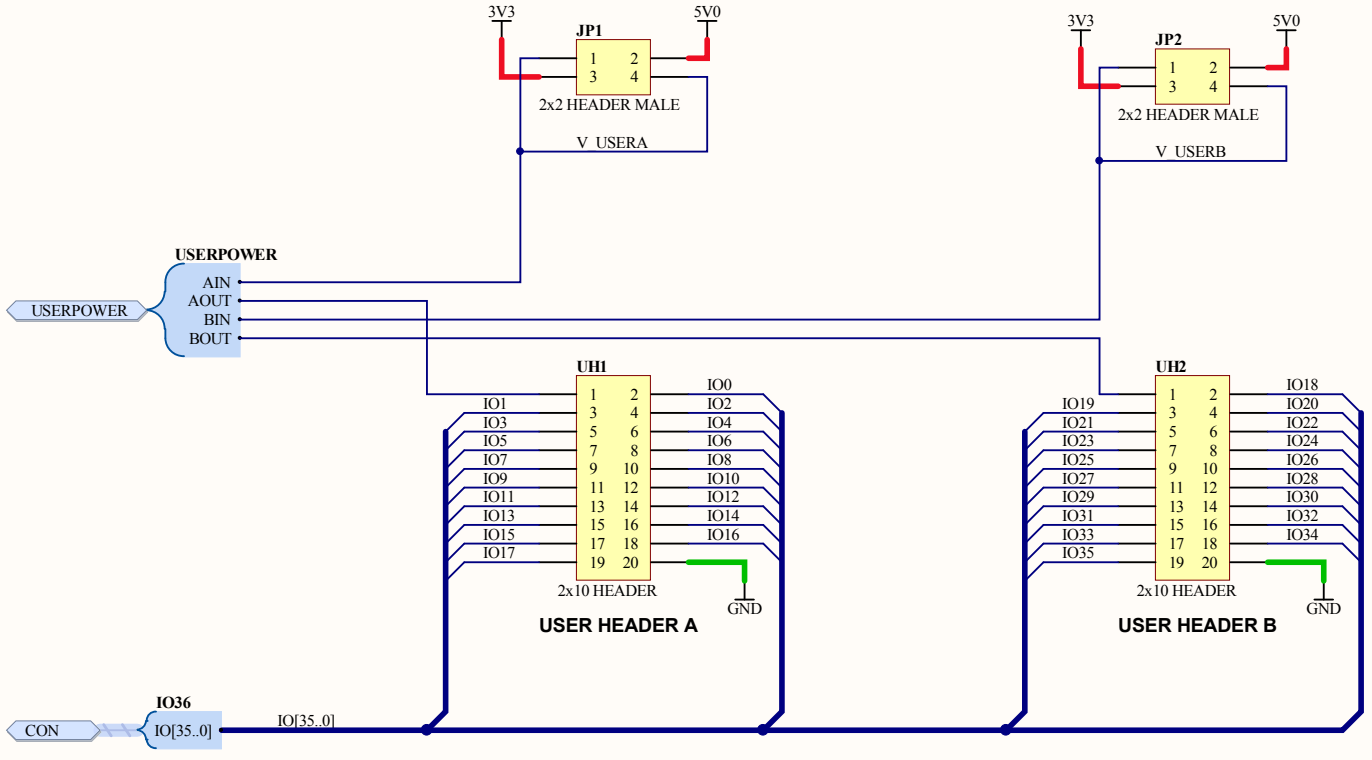

Sheet Title	*36-Way User I/O Headers*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:26 PM	Sheet 50 of 80	
File: CON_USER_20WBOXHDRRAMx2.SCHDOC			

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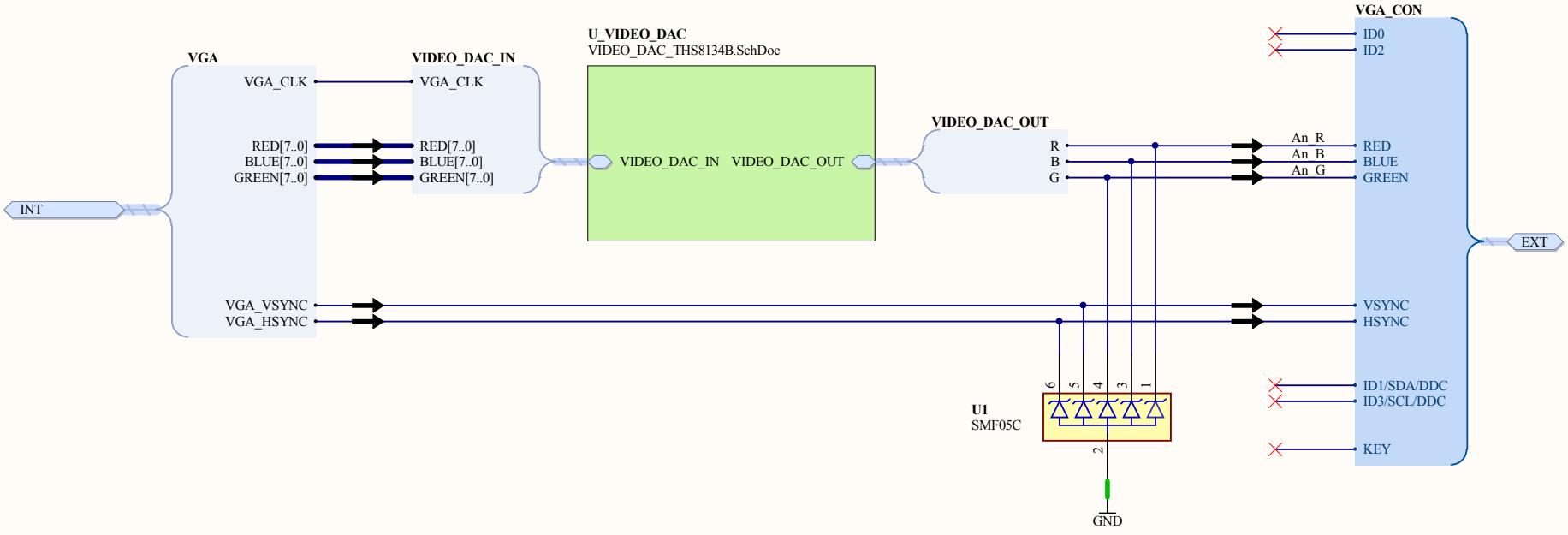

Sheet Title	*VGA Ouput*	
Project Title	*NB3000XN - Xilinx*	
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010	Time: 5:40:26 PM	Sheet 51 of 80
File: VGA_OUT.SCHDOC		

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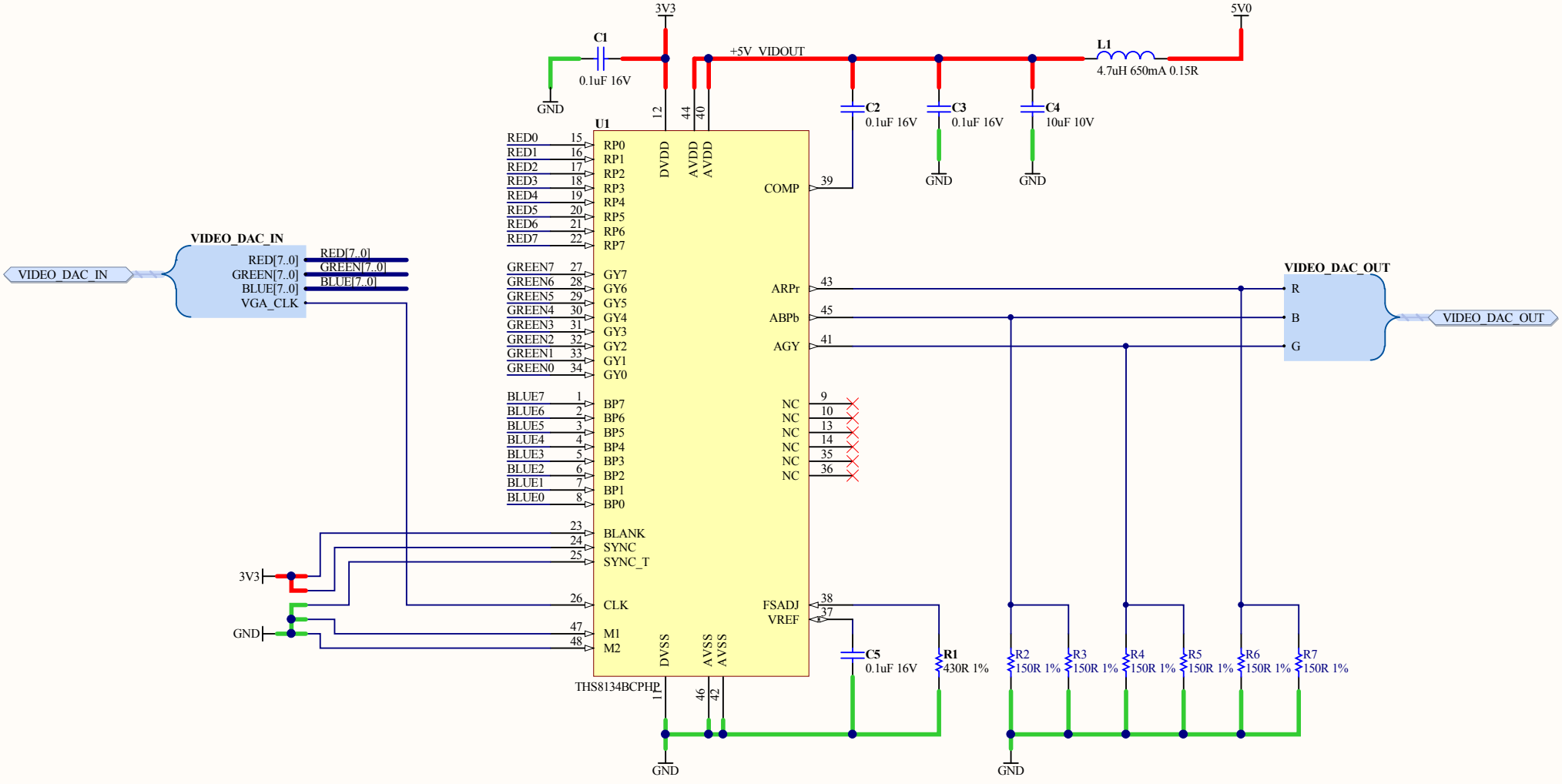

Sheet Title	*Video DAC*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:26 PM	Sheet 52 of 80	
File: VIDEO_DAC_THS8134B.SchDoc			

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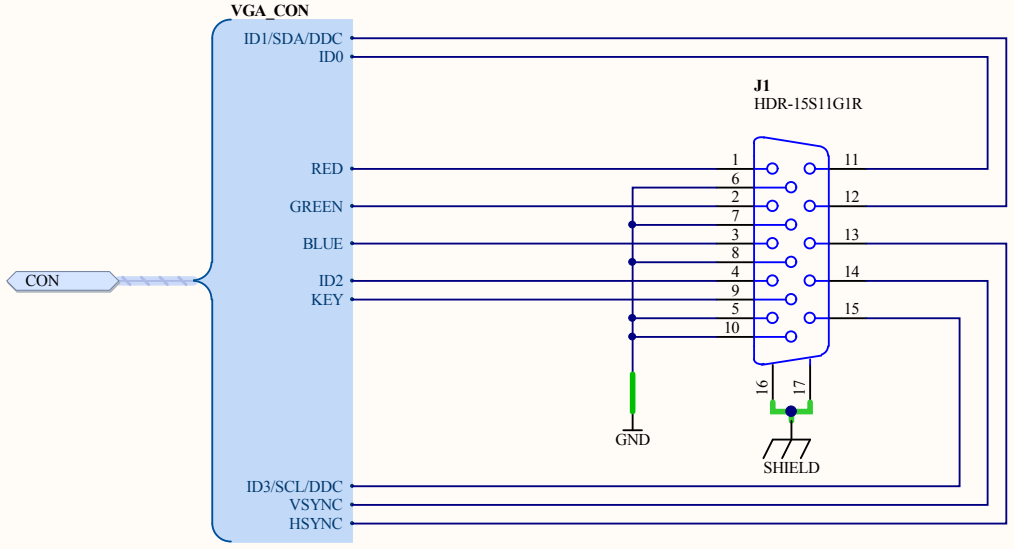

SVGA INTERFACE

Sheet Title	*Video Out Connector*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 53 of 80	
File: CON_VGA_DB15.SCHDOC			

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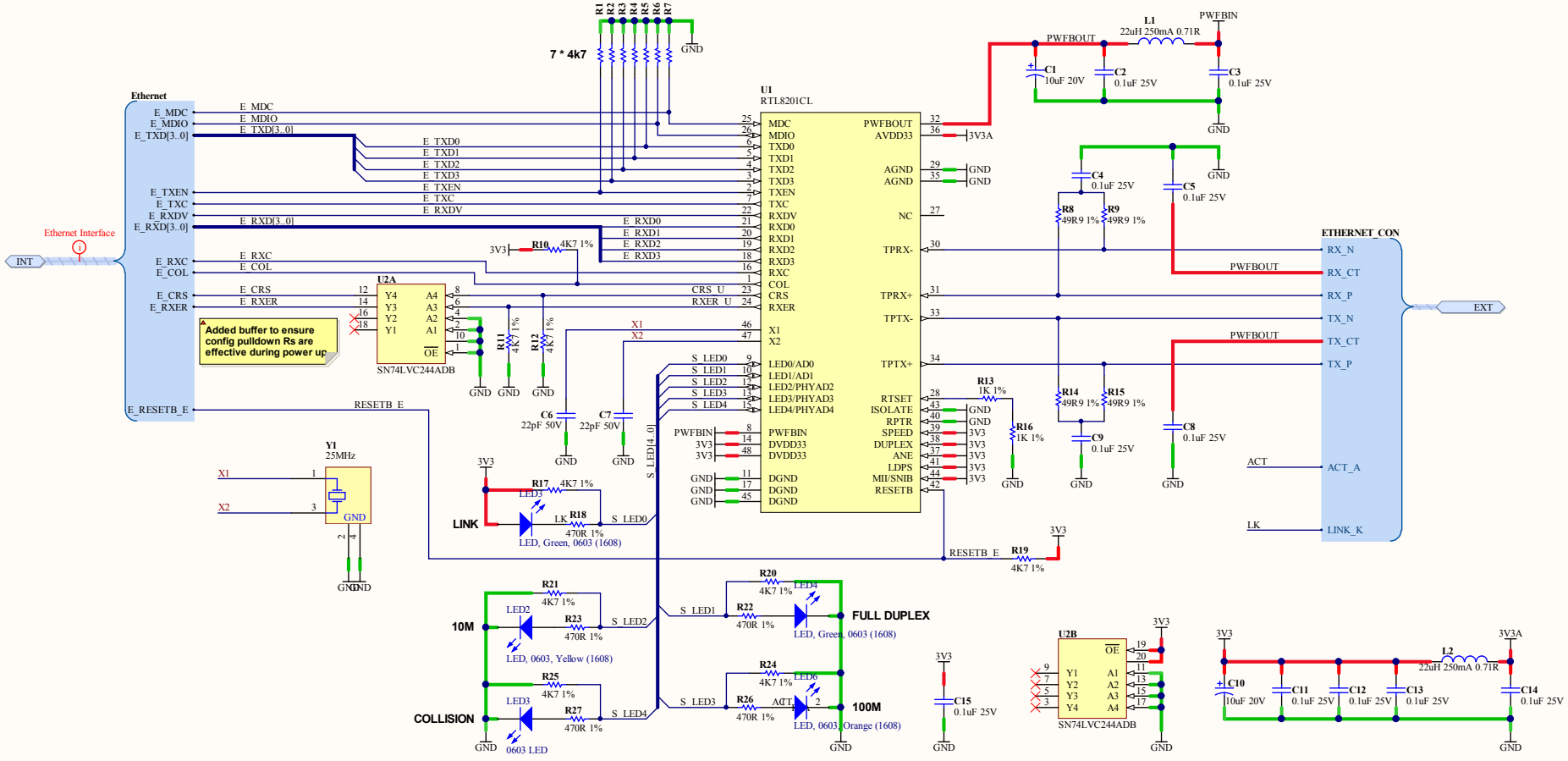

Sheet Title	*Ethernet Interface*		
Project Title	*NB3000XN - Xilinx*		
Size: A3	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 54 of 80	
File: Ethernet_RTL8201CL.SchDoc			

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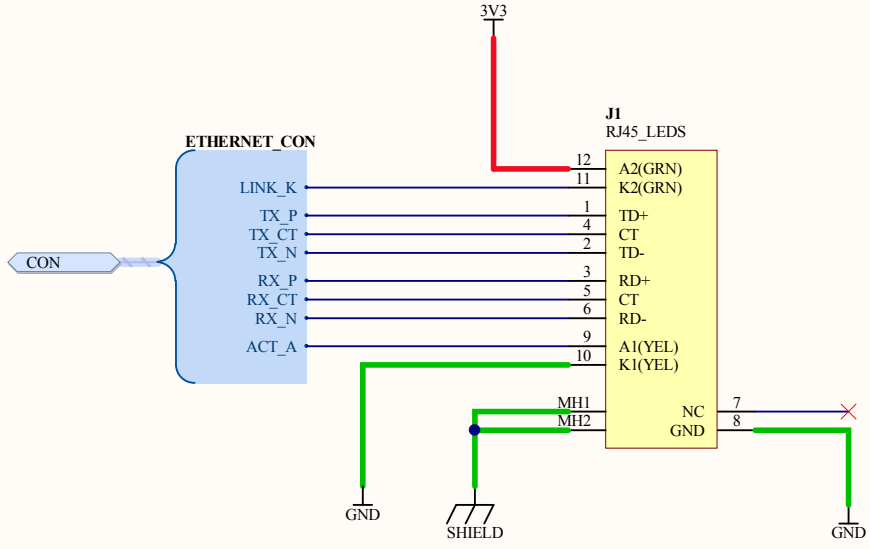

Sheet Title	***Ethernet Connector***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 55 of 80	
File: CON_ETHERNET_RJ45_LEDS.SchDoc			

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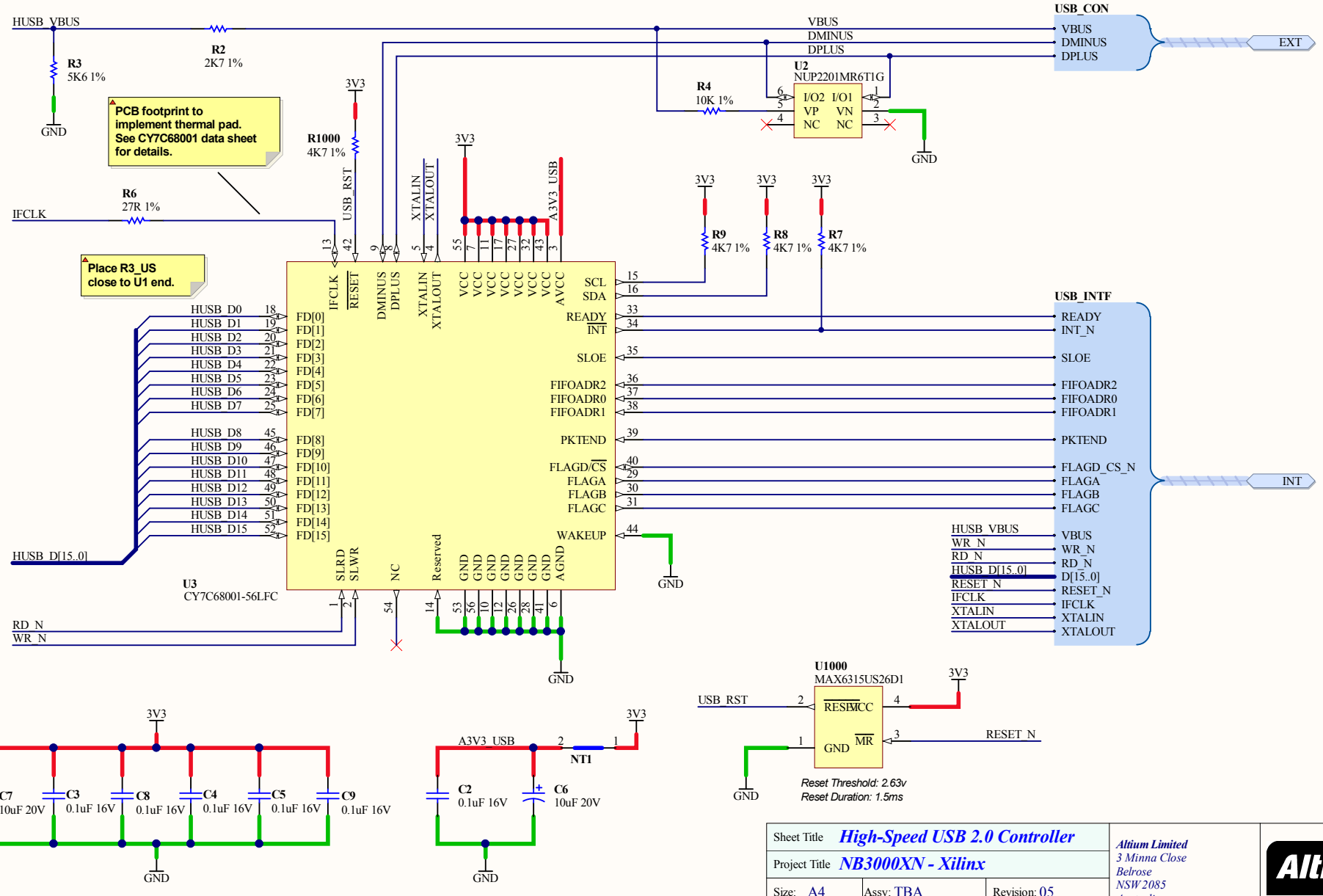
HUSB_VBUS
R3
5K6 1%
GND
R2
2K7 1%
PCB footprint to implement thermal pad. See CY7C68001 data sheet for details.
3V3
R1000
4K7 1%
USB_RST
R6
27R 1%
IFCLK
Place R3_US close to U1 end.
XTALIN
XTALOUT
A3V3_USB
R4
10K 1%
U2
NUP2201MR6T1G
I/O2 I/O1
VP VN
NC NC
VBUS
DMINUS
DPLUS
USB_CON
EXT
R9
4K7 1%
R8
4K7 1%
R7
4K7 1%
HUSB_D0
HUSB_D1
HUSB_D2
HUSB_D3
HUSB_D4
HUSB_D5
HUSB_D6
HUSB_D7
HUSB_D8
HUSB_D9
HUSB_D10
HUSB_D11
HUSB_D12
HUSB_D13
HUSB_D14
HUSB_D15
HUSB_D[15..0]
FD[0]
FD[1]
FD[2]
FD[3]
FD[4]
FD[5]
FD[6]
FD[7]
FD[8]
FD[9]
FD[10]
FD[11]
FD[12]
FD[13]
FD[14]
FD[15]
IFCLK
RESET
DMINUS
DPLUS
XTALIN
XTALOUT
VCC
AVCC
SCL
SDA
READY
INT
SLOE
FIFOADR2
FIFOADR0
FIFOADR1
PKTEND
FLAGD/CS
FLAGA
FLAGB
FLAGC
WAKEUP
SLRD
SLWR
NC
Reserved
GND
AGND
U3
CY7C68001-56LFC
RD_N
WR_N
USB_INTF
READY
INT_N
SLOE
FIFOADR2
FIFOADR0
FIFOADR1
PKTEND
FLAGD_CS_N
FLAGA
FLAGB
FLAGC
INT
HUSB_VBUS
WR_N
RD_N
HUSB_D[15..0]
RESET_N
IFCLK
XTALIN
XTALOUT
VBUS
D[15..0]
RESET_N
U1000
MAX6315US26D1
USB_RST
RESET
VCC
GND
MR
RESET_N
Reset Threshold: 2.63v
Reset Duration: 1.5ms
C7
10uF 20V
C3
0.1uF 16V
C8
0.1uF 16V
C4
0.1uF 16V
C5
0.1uF 16V
C9
0.1uF 16V
C2
0.1uF 16V
C6
10uF 20V
NT1
Sheet Title High-Speed USB 2.0 Controller
Project Title NB3000XN - Xilinx
Size: A4
Assy: TBA
Revision: 05
Date: 28/01/2010
Time: 5:40:27 PM
Sheet 56 of 80
File: USB_CY7C68001-56LFC.SchDoc
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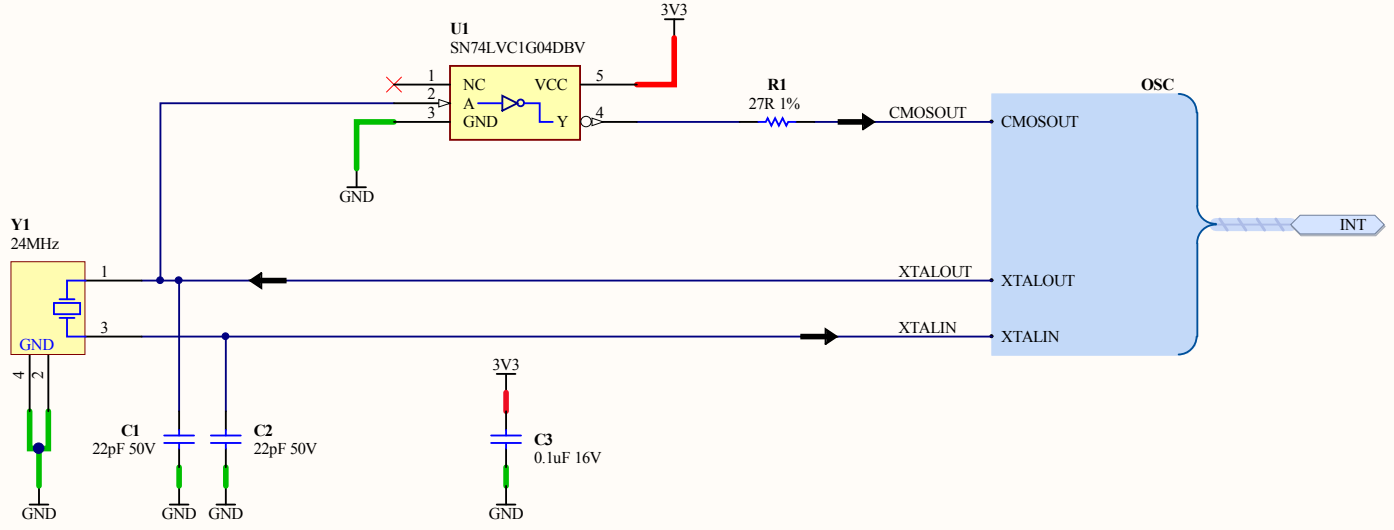

Sheet Title	*24MHz Oscillator*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 57 of 80	
File: OSC_24MHZ.SchDoc			

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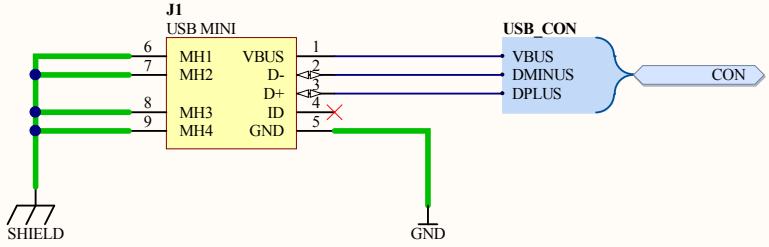

Sheet Title	***USB 2.0 Type B Connector***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 58 of 80	
File: CON_MINI_USBB_RA_KME04-USBMU03A01-1.SchDoc			

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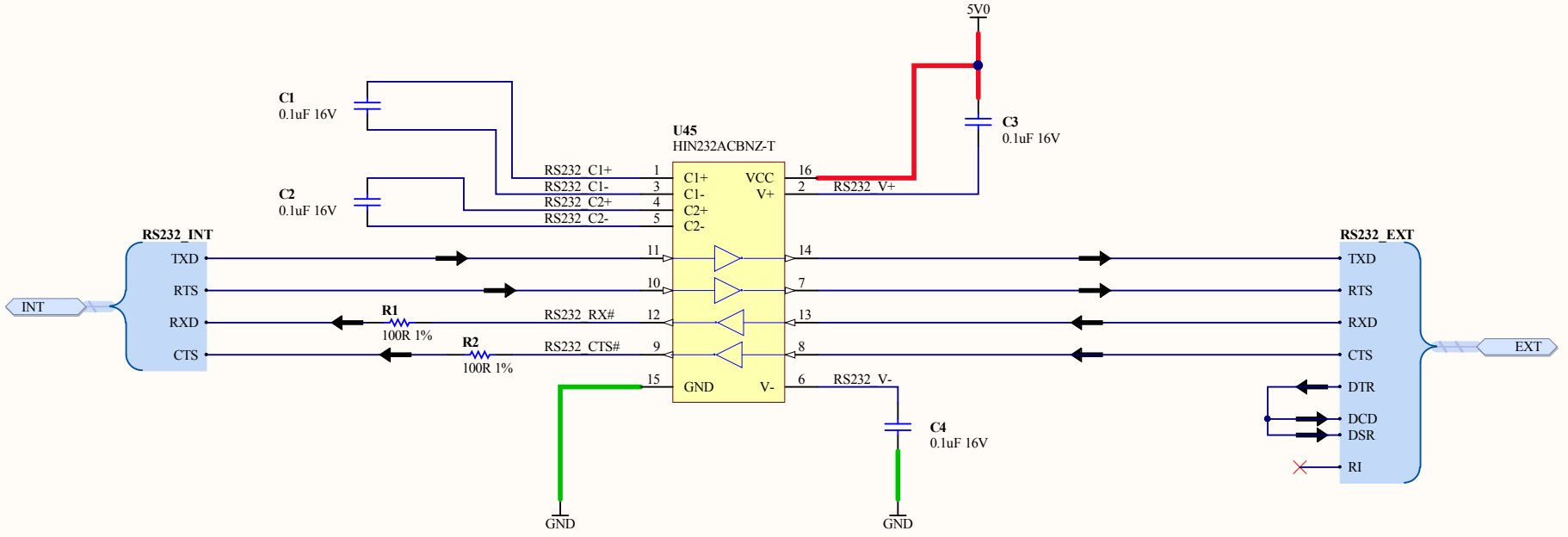

Sheet Title	*RS232 Communication IC*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 59 of 80	
File: RS232_HIN232.SchDoc			

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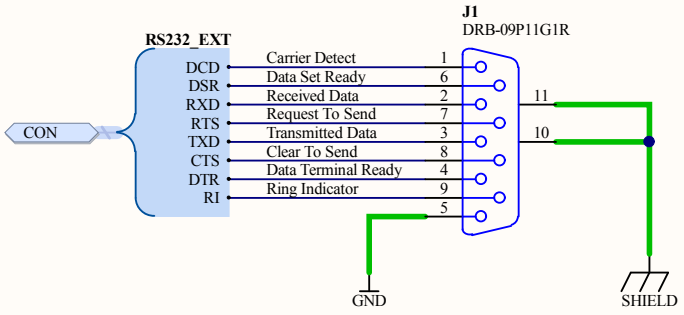

RS232 DB-9 Male Connector
EIA-574 Standard

Sheet Title	***RS232-DCE DB9***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 60 of 80	
File: CON_RS232DCE_DB9_TH.SchDoc			

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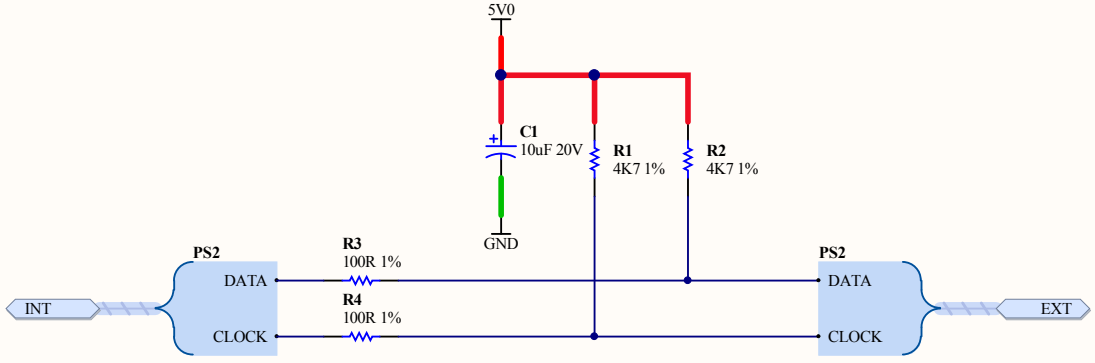

Sheet Title	*PC PS2*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:27 PM	Sheet 61 of 80	
File: PC_PS2.SchDoc			

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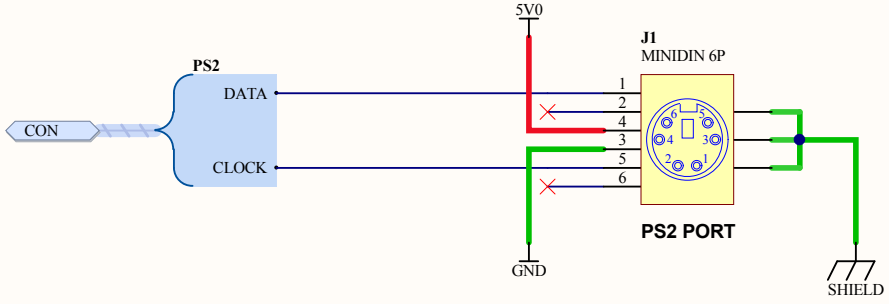

Sheet Title	*PS2 MINIDIN6F Connector (Black)*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 62 of 80	
File: CON_PS2PORT_MINIDIN6F_BLACK.SchDoc			

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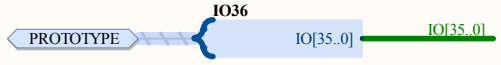

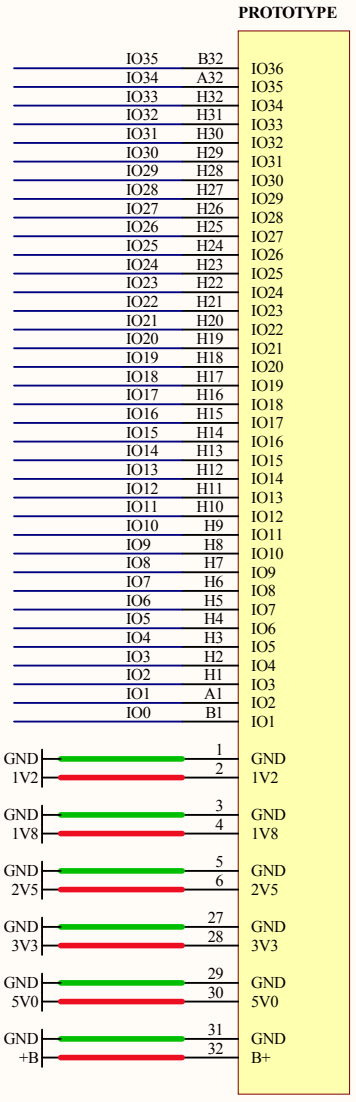

Sheet Title	*User Prototyping Area*	
Project Title	*NB3000XN - Xilinx*	
Size: A4	Assy: TBA	Revision: 05
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 63 of 80
File: PROTOTYPE A.SchDoc		

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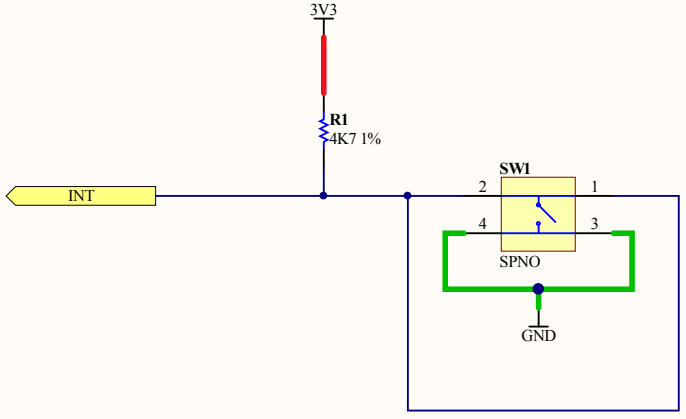

Sheet Title	***Push Button SPNO Switch***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 64 of 80	
File: SW_RESET_SPNO.SCHDOC			

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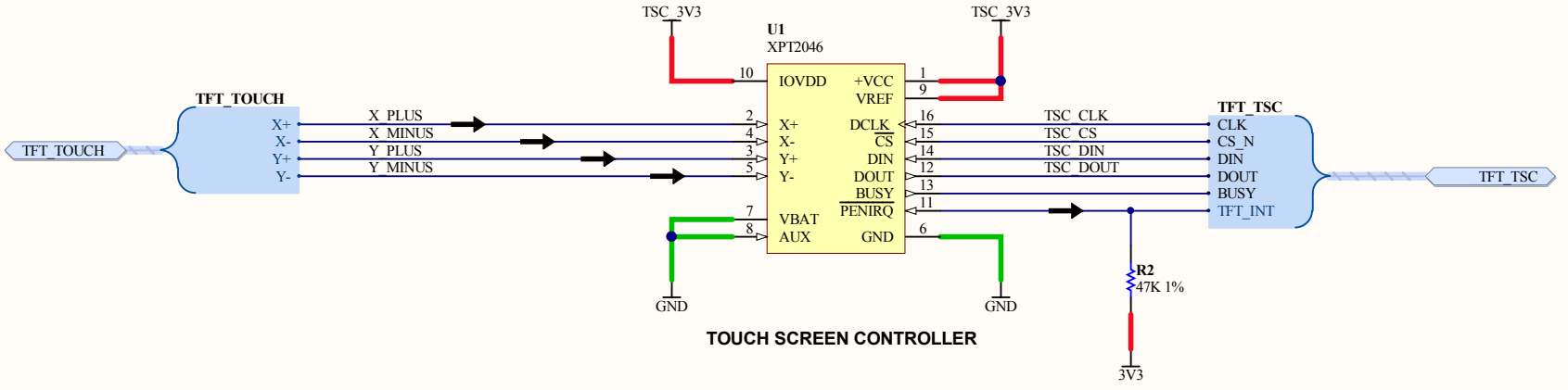

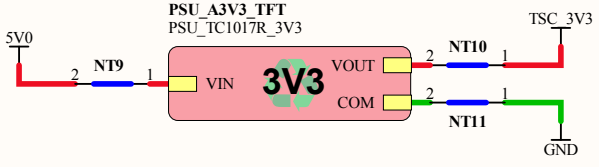

Sheet Title	*TFT Touchscreen Interface*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 65 of 80	
File: TSC_XPT2046.SchDoc			

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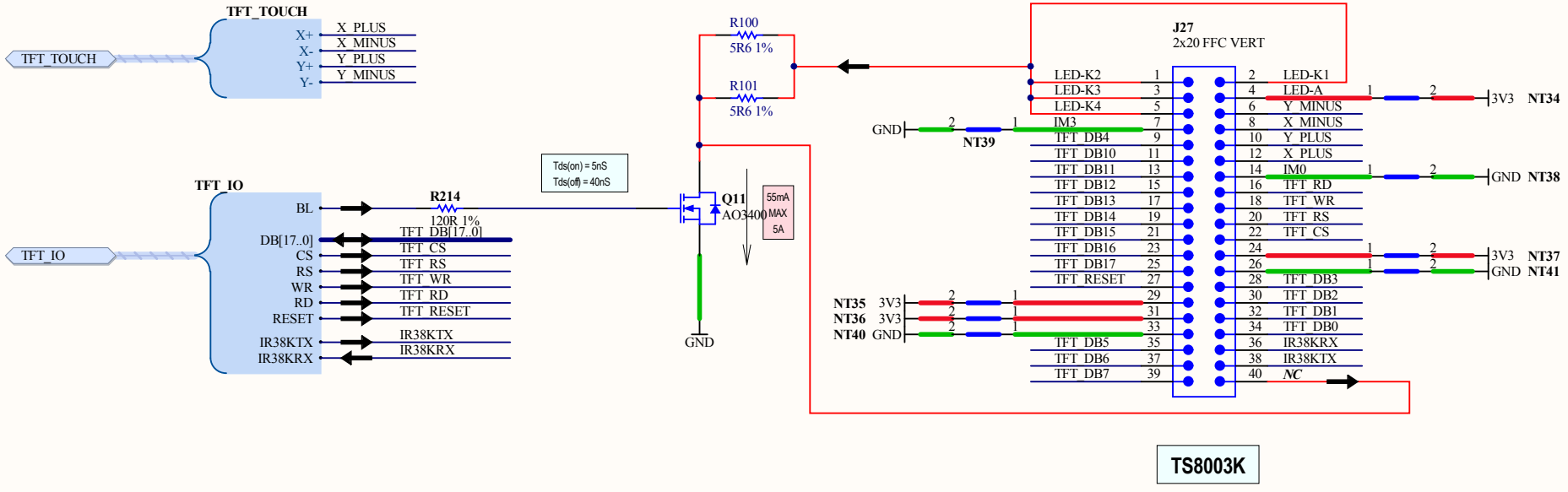

Sheet Title	*LCD Module Connector*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 66 of 80	
File: CON_FFC40_LCDTFT.SCHDOC			

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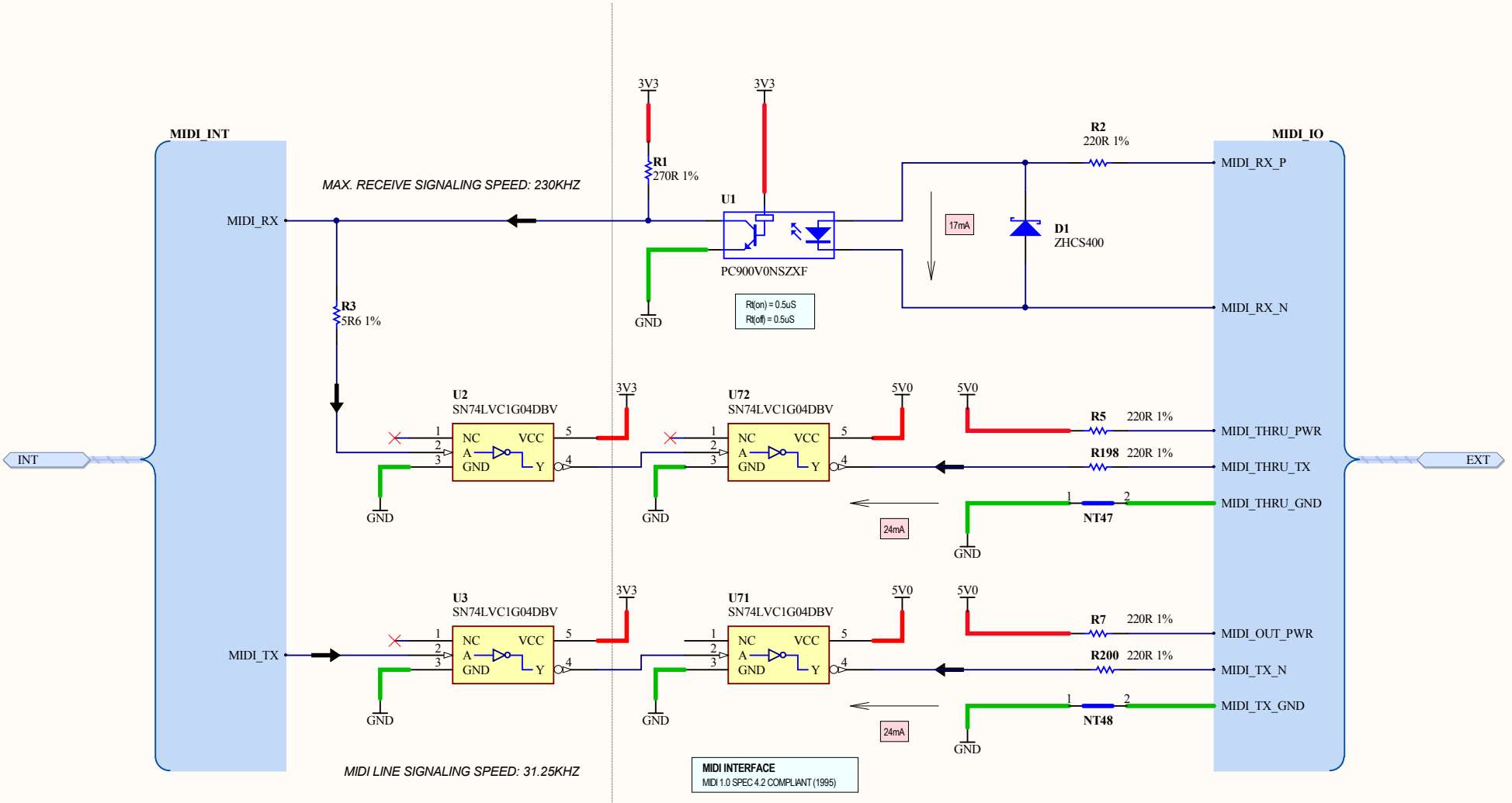

Sheet Title	*MIDI Sub-system*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 67 of 80	
File: MIDI_FULL.SCHDOC			

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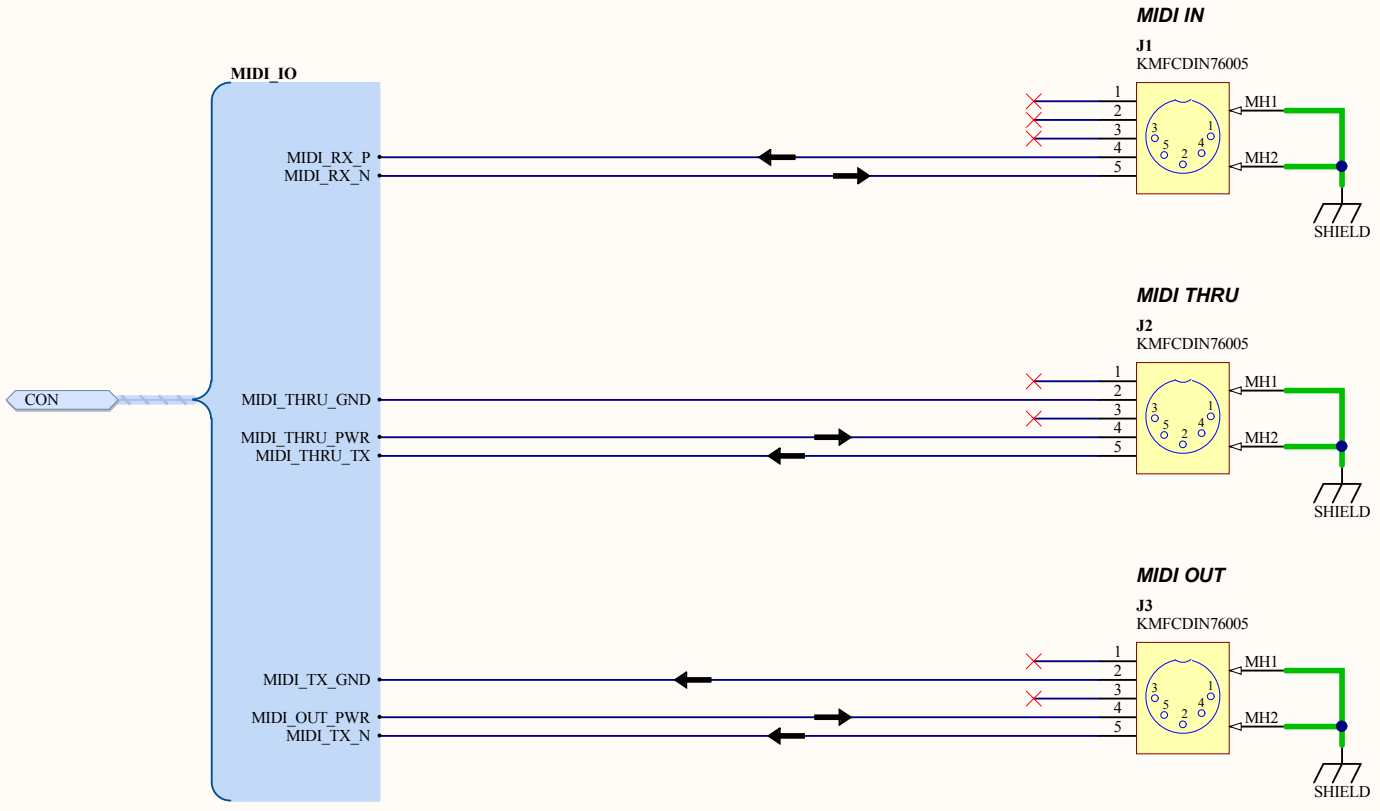

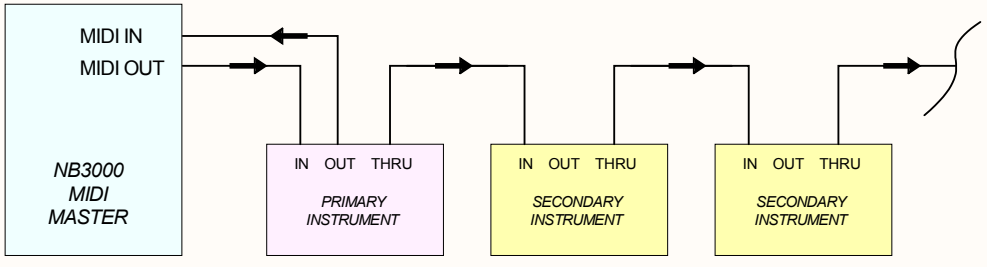

Sheet Title	*MIDI Connectors*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 68 of 80	
File: CON_MIDI_DIN5.SCHDOC			

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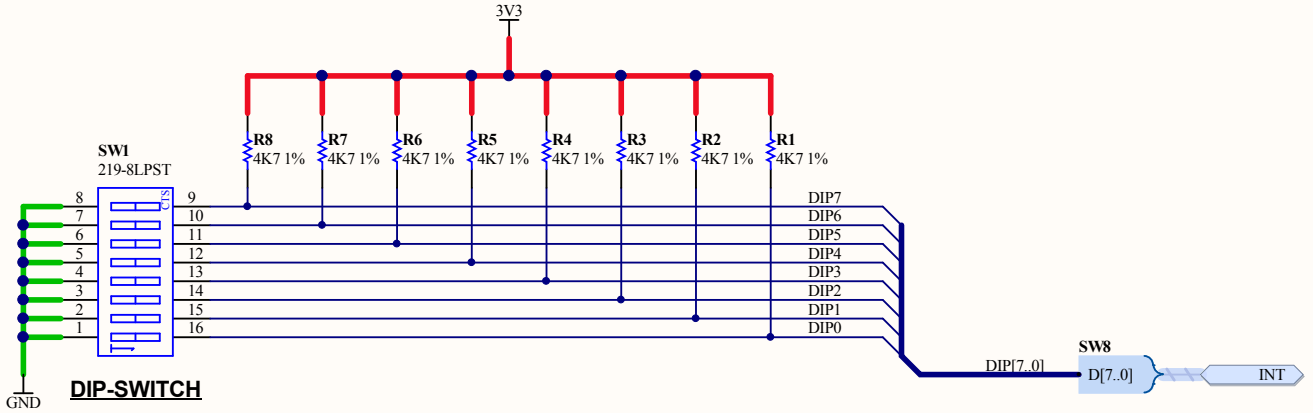

Sheet Title	*8-Way SPST DIP Switch (SMT)*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 69 of 80	
File: SW_DIP8_SMT.SchDoc			

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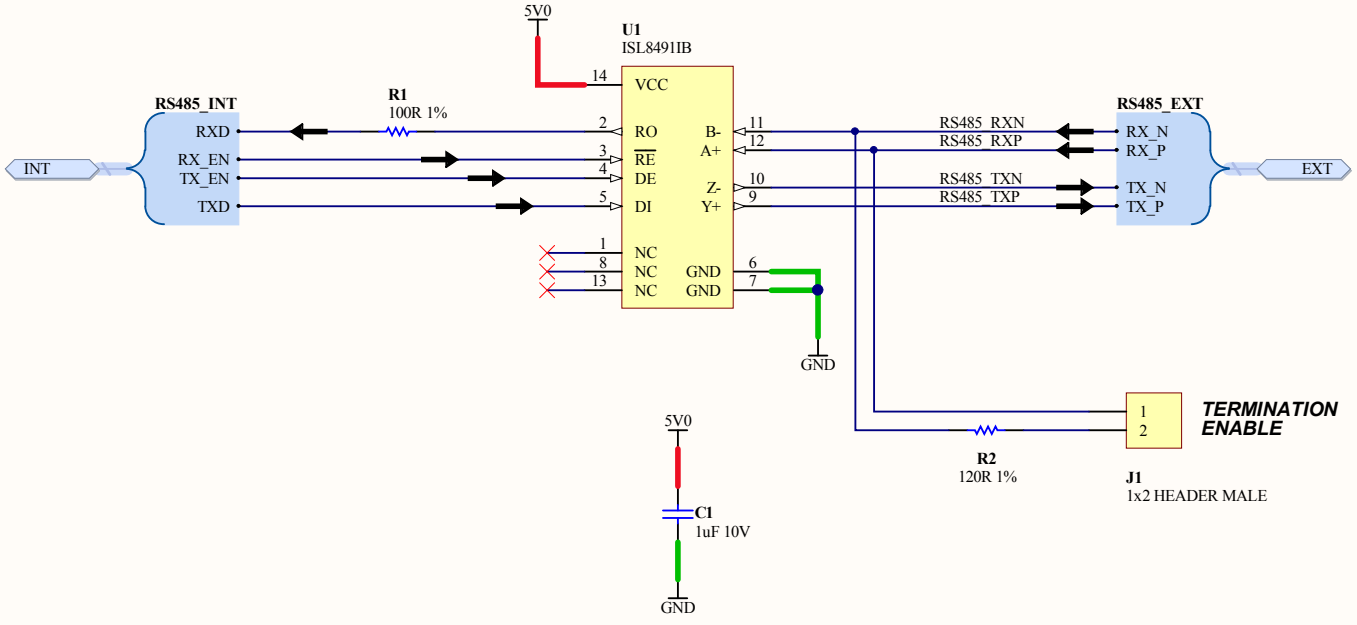

Sheet Title	*RS485 Communication IC*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:28 PM	Sheet 70 of 80	
File: RS485_ISL8491.SchDoc			

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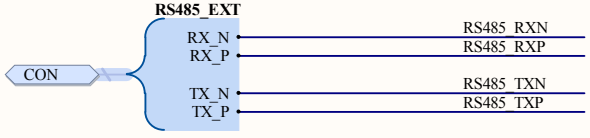

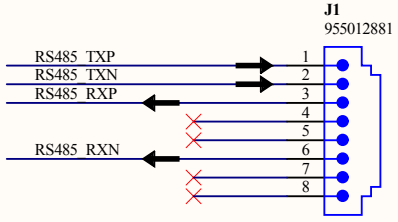

Sheet Title	***RS485 Connector***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:29 PM	Sheet 71 of 80	
File: CON_RS485_RJ45.SchDoc			

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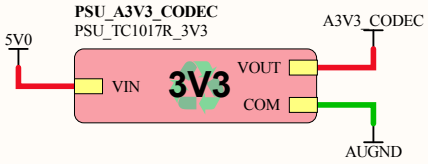

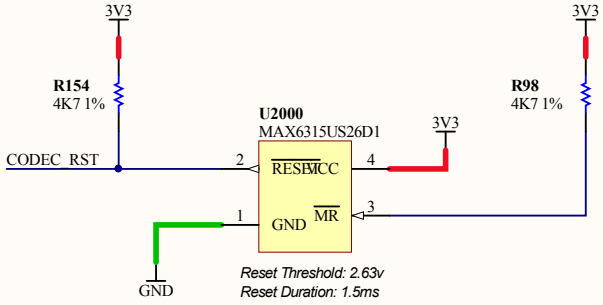

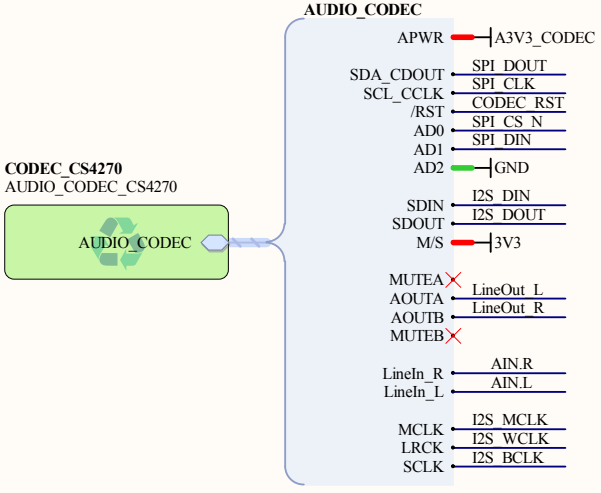

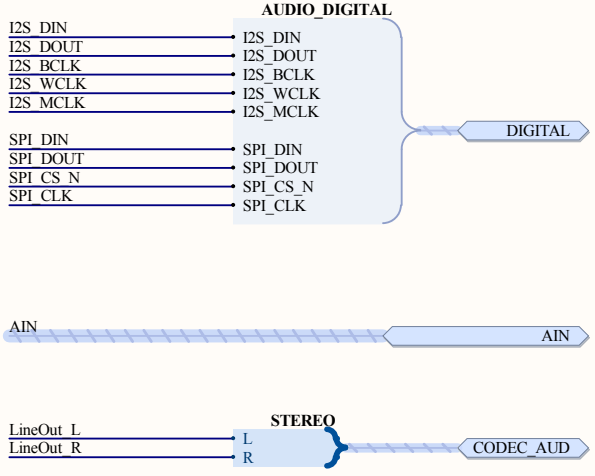

Sheet Title	*Audio CODEC*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:29 PM	Sheet 72 of 80	
File: Audio_Codec.SchDoc			

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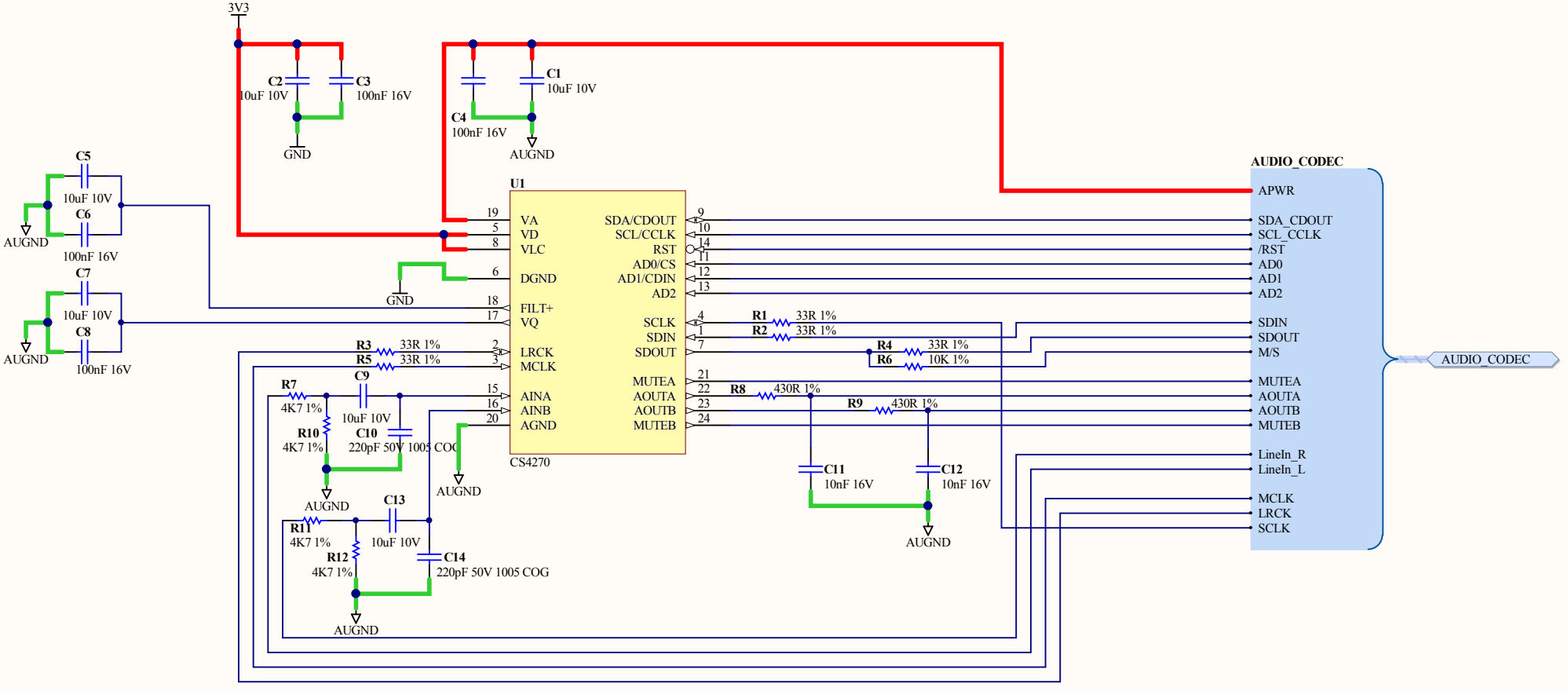

Sheet Title	*Audio CODEC*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:29 PM	Sheet 73 of 80	
File: AUDIO_CODEC_CS4270.SchDoc			

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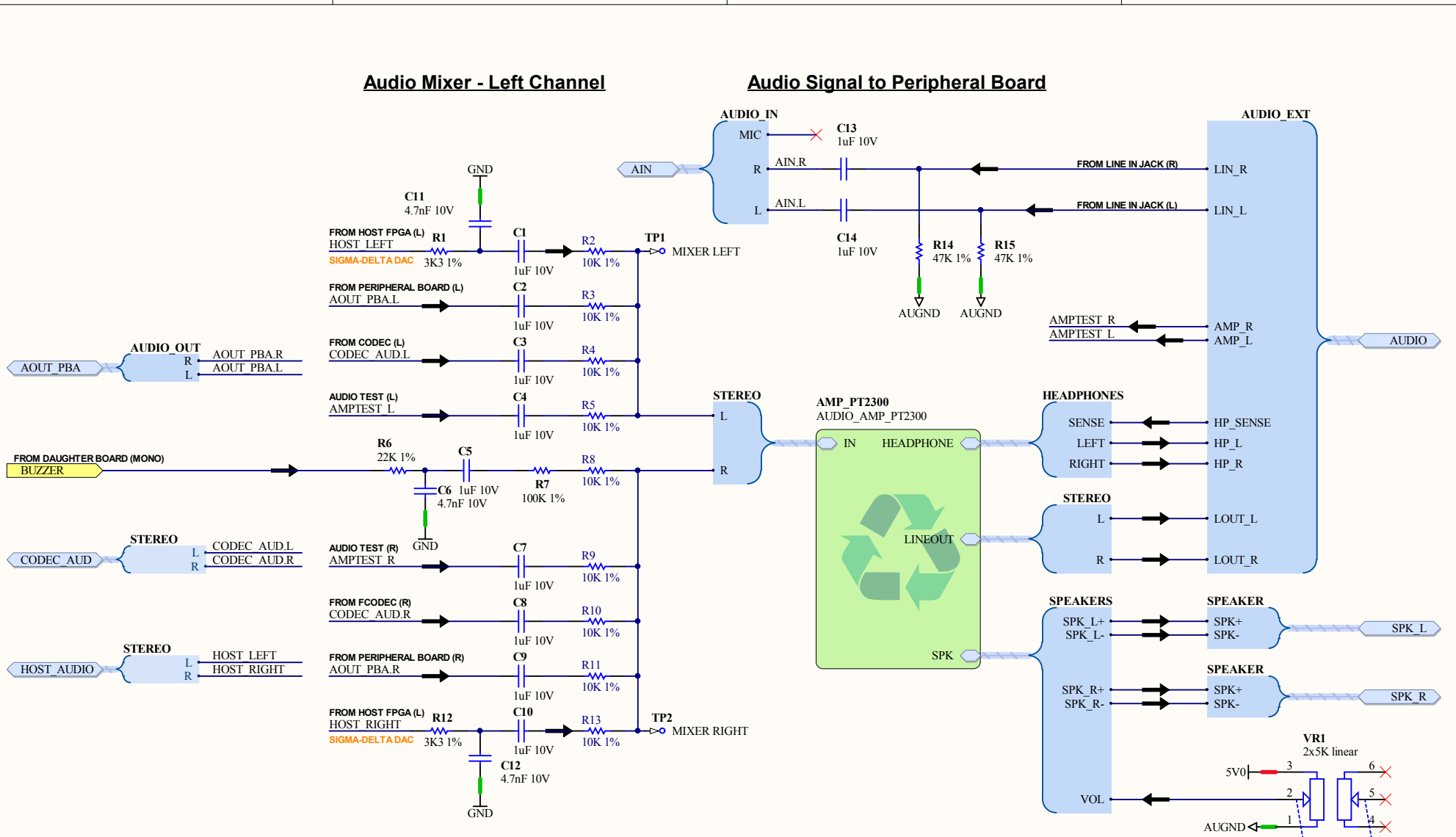
Audio Mixer - Left Channel
Audio Signal to Peripheral Board
AUDIO_IN
MIC
R
L
AIN
AIN.R
AIN.L
C13
1uF 10V
C14
1uF 10V
R14
47K 1%
R15
47K 1%
AUGND
AUGND
AUDIO_EXT
FROM LINE IN JACK (R)
FROM LINE IN JACK (L)
LIN_R
LIN_L
AMPTEST_R
AMPTEST_L
AMP_R
AMP_L
AUDIO
GND
C11
4.7nF 10V
FROM HOST FPGA (L)
HOST_LEFT
SIGMA-DELTA DAC
R1
3K3 1%
C1
1uF 10V
R2
10K 1%
TP1
MIXER LEFT
FROM PERIPHERAL BOARD (L)
AOUT_PBA.L
C2
1uF 10V
R3
10K 1%
AUDIO_OUT
AOUT_PBA
R
L
AOUT_PBA.R
AOUT_PBA.L
FROM CODEC (L)
CODEC_AUD.L
C3
1uF 10V
R4
10K 1%
AUDIO TEST (L)
AMPTEST_L
C4
1uF 10V
R5
10K 1%
STEREO
L
R
AMP_PT2300
AUDIO_AMP_PT2300
IN
HEADPHONE
LINEOUT
SPK
HEADPHONES
SENSE
LEFT
RIGHT
HP_SENSE
HP_L
HP_R
STEREO
L
R
LOUT_L
LOUT_R
FROM DAUGHTER BOARD (MONO)
BUZZER
R6
22K 1%
C5
C6 1uF 10V
4.7nF 10V
R7
100K 1%
R8
10K 1%
GND
STEREO
CODEC_AUD
L
R
CODEC_AUD.L
CODEC_AUD.R
AUDIO TEST (R)
AMPTEST_R
C7
1uF 10V
R9
10K 1%
FROM FCODEC (R)
CODEC_AUD.R
C8
1uF 10V
R10
10K 1%
SPEAKERS
SPK_L+
SPK_L-
SPK_R+
SPK_R-
SPEAKER
SPK+
SPK-
SPK_L
SPK_R
STEREO
HOST_AUDIO
L
R
HOST_LEFT
HOST_RIGHT
FROM PERIPHERAL BOARD (R)
AOUT_PBA.R
C9
1uF 10V
R11
10K 1%
FROM HOST FPGA (L)
HOST_RIGHT
SIGMA-DELTA DAC
R12
3K3 1%
C10
1uF 10V
R13
10K 1%
TP2
MIXER RIGHT
C12
4.7nF 10V
GND
VR1
2x5K linear
5V0
VOL
AUGND
Audio Mixer - Right Channel
Sheet Title AUDIO SUB-SYSTEM
Project Title NB3000XN - Xilinx
Size: A4
Assy: TBA
Revision: 05
Date: 28/01/2010
Time: 5:40:29 PM
Sheet 74 of 80
File: AUDIO_AMP_NB2C.SchDoc
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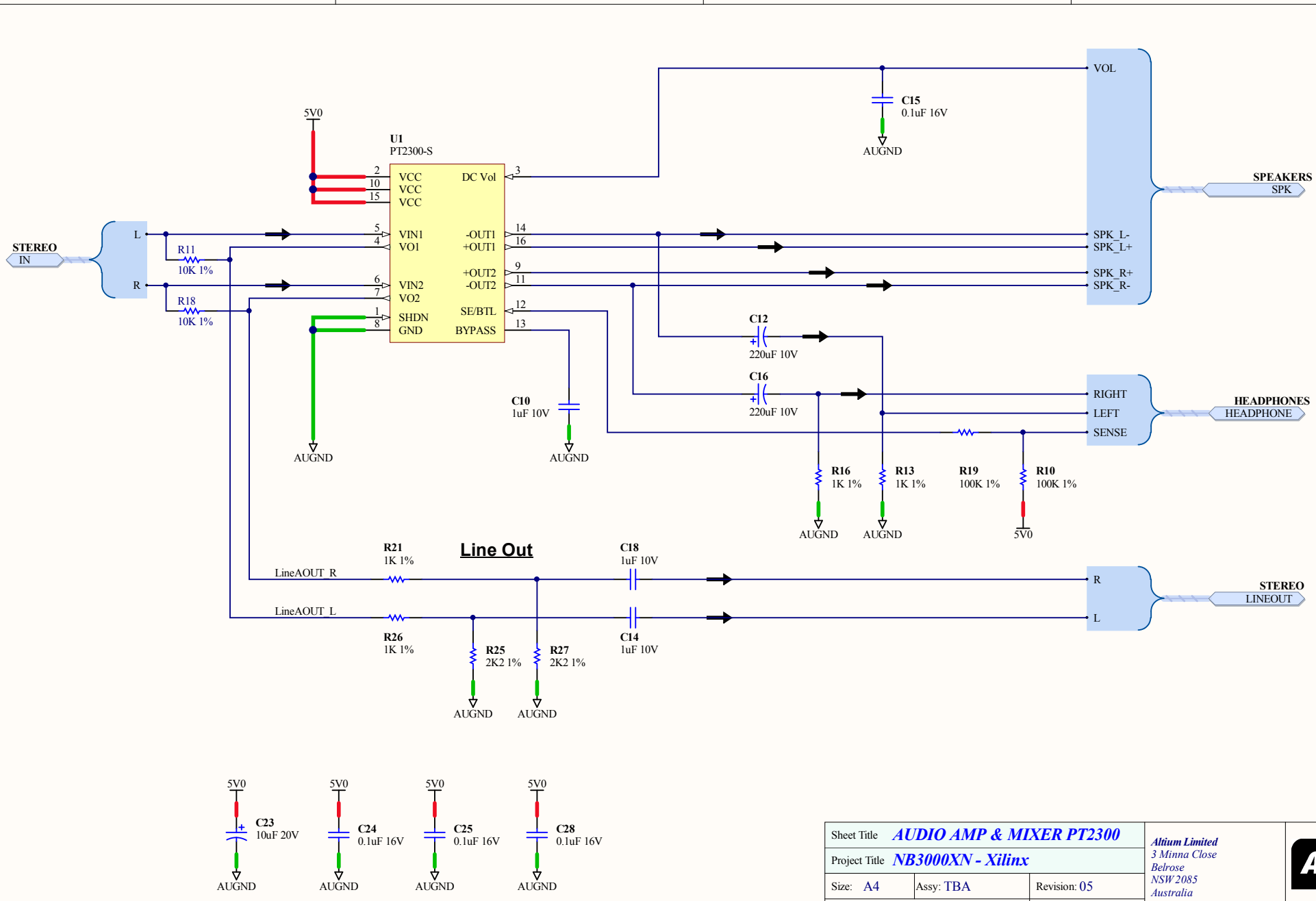

Sheet Title	*AUDIO AMP & MIXER PT2300*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:29 PM	Sheet 75 of 80	
File: AUDIO_AMP_PT2300.SchDoc			

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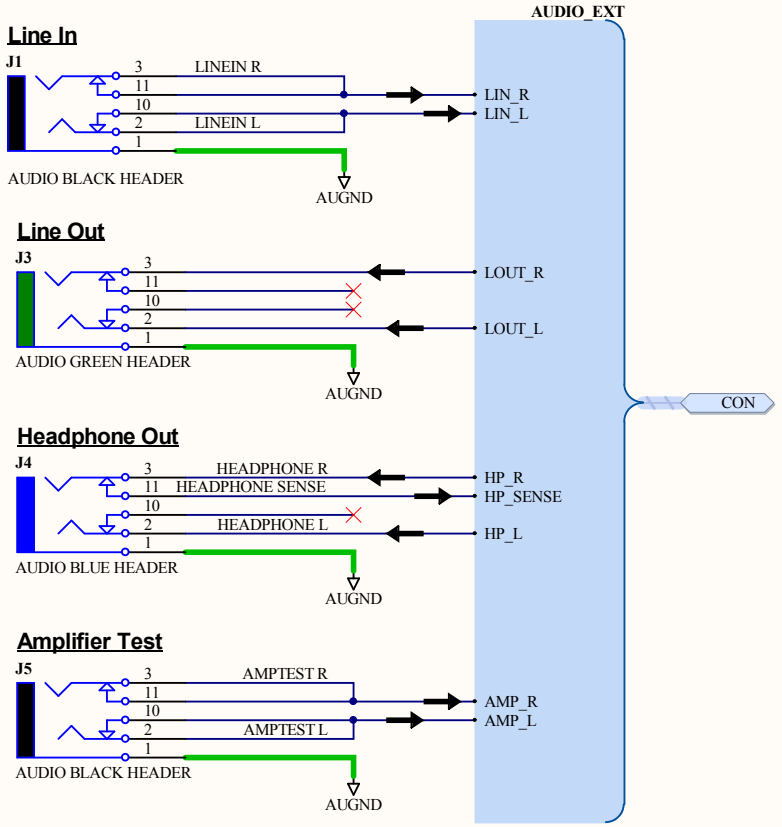

Sheet Title	*AUDIO AC99 Interface*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:29 PM	Sheet 76 of 80	
File: CON_AUDIO_AC99_NOMIC.SchDoc			

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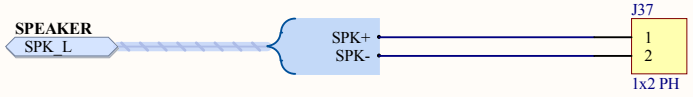
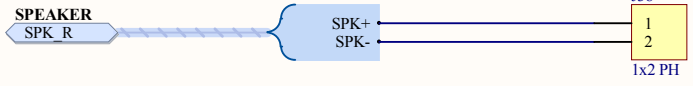


External Speakers Left



External Speakers Right

Sheet Title	***External Speaker Connectors***		
Project Title	***NB3000XN - Xilinx***		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:29 PM	Sheet 77 of 80	
File: CON_EXT_SPK.SchDoc			

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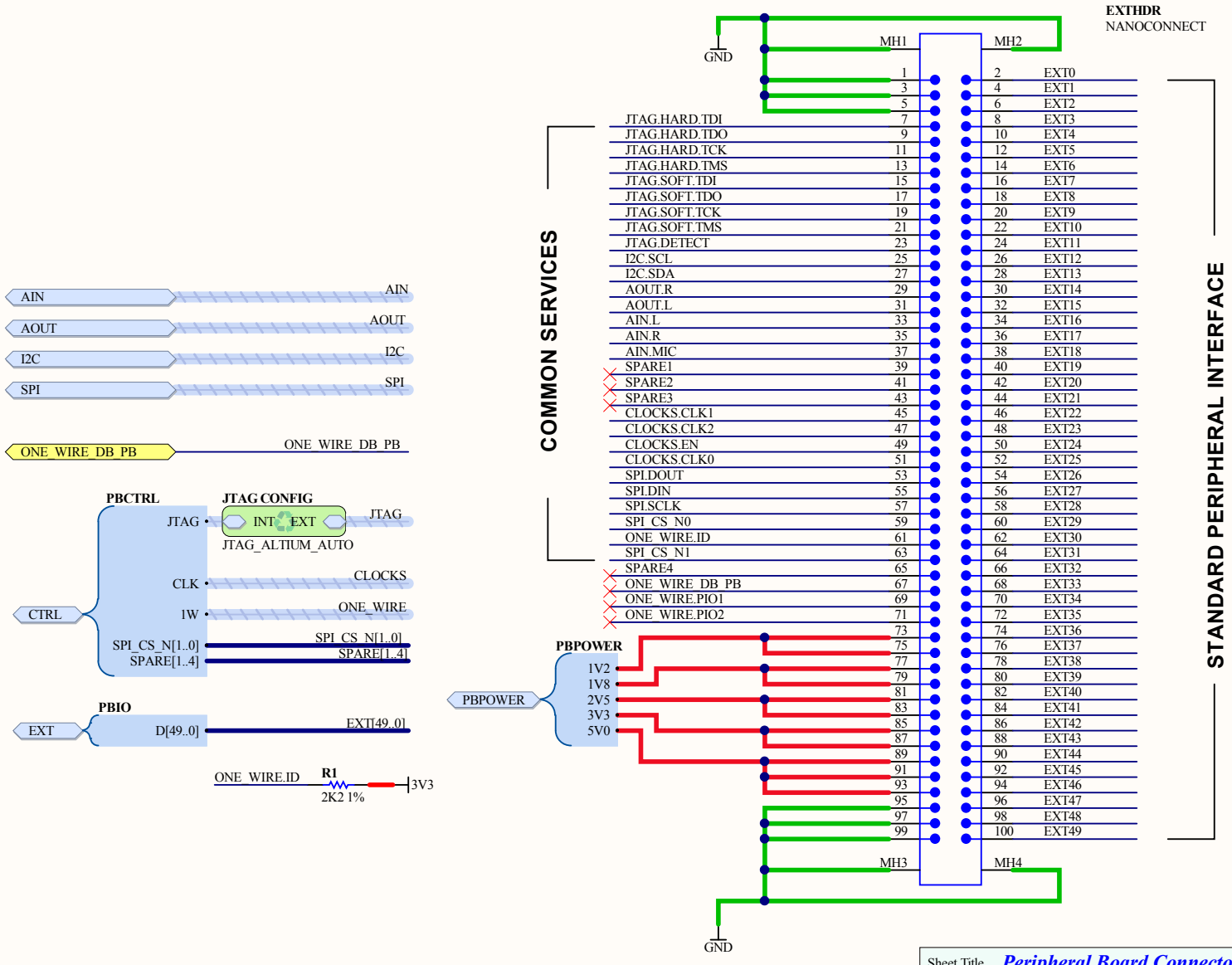

Sheet Title	*Peripheral Board Connector*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:29 PM	Sheet 78 of 80	
File: PBCON.schdoc			

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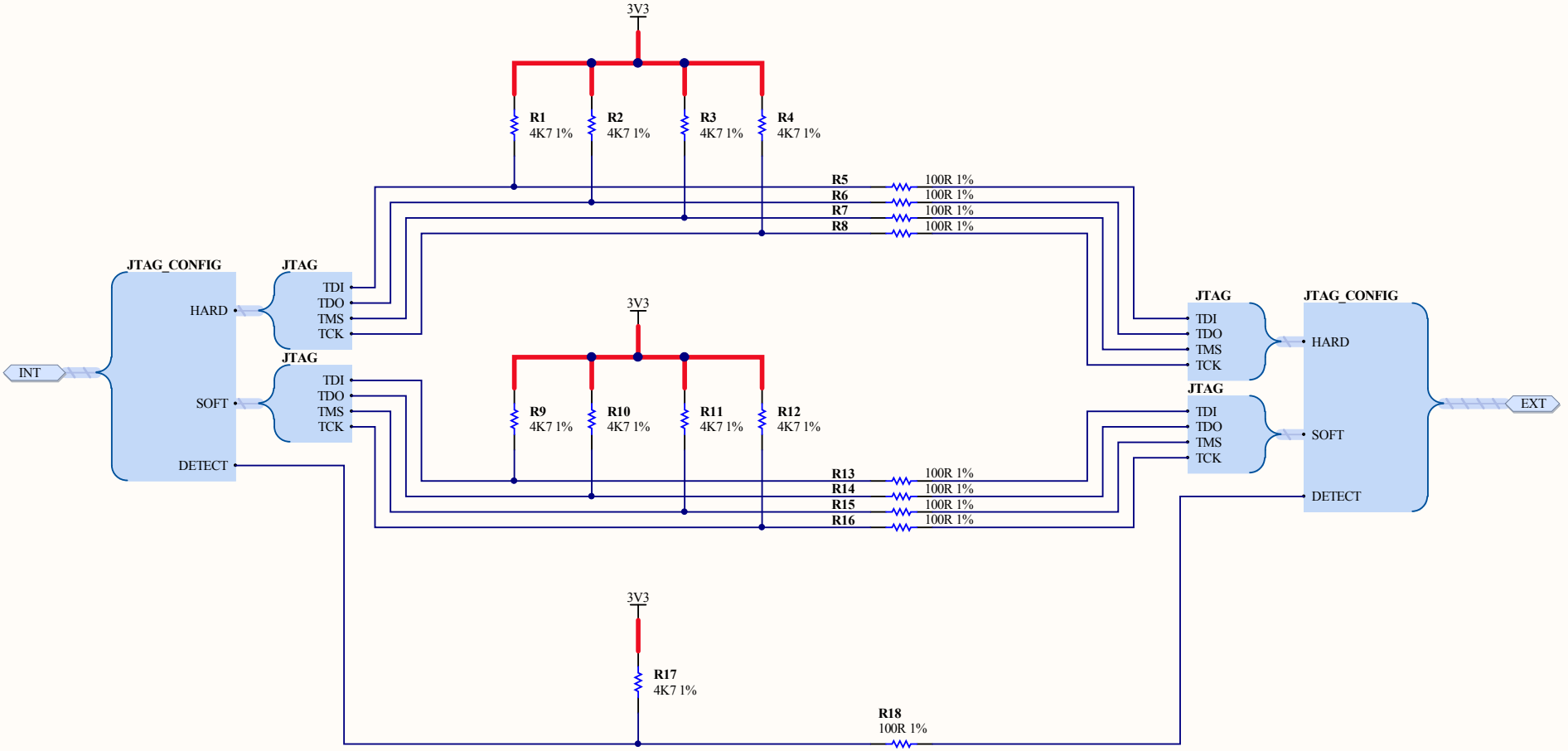

Sheet Title	*Auto-Detect JTAG Circuit*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:30 PM	Sheet 79 of 80	
File: JTAG_ALTIUM_AUTO.SchDoc			

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Standoffs For Peripheral Board

PB_MH1
8.5mm spacer, Gold, 2xM3

PB_MH2
8.5mm spacer, Gold, 2xM3

PB_MH3
8.5mm spacer, Gold, 2xM3

PB_MH4
8.5mm spacer, Gold, 2xM3

PB_MH5
8.5mm spacer, Gold, 2xM3

Fiducial Alignment Components

FD1
Fiducial - Round

FD2
Fiducial - Round

FD3
Fiducial - Round

PCB1
NB3000XN Blank PCB
Printed Circuit Board (Bare)

PCB Identifiers

Altium Logo BOT1
Altium(2009)

LOGO1
Nanoboard Logo

Sheet Title	*NB3000XN Holes and Graphics*		
Project Title	*NB3000XN - Xilinx*		
Size: A4	Assy: TBA	Revision: 05	
Date: 28/01/2010	Time: 5:40:30 PM	Sheet 80 of 80	
File: Mounts.SchDoc			

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